MRF24J40
Data Sheet

IEEE 802.15.4™ 2.4 GHz RF Transceiver
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ISO/TS 16949:2002
MRF24J40

IEEE 802.15.4™ 2.4 GHz RF Transceiver

Devices Included:
- MRF24J40

Features:
- Complete IEEE 802.15.4 Specification Compliant
- Supports MIWi™, ZigBee™ and Proprietary Protocols
- Simple, 4-Wire SPI Interface
- Integrated 20 MHz and 32.768 kHz Oscillator Drive
- 20 MHz Reference Clock Output:
  - Available to drive microcontroller oscillator
- Supports Power-Saving mode
- Low-Current Consumption, Typical 18 mA in RX mode and 22 mA in TX mode
- Typical 2 μA Sleep mode
- Small, 40-Pin Leadless QFN 6x6 mm² Package

RF/Analog Features:
- ISM Band 2.405-2.48 GHz Operation
- -91 dBm Typical Sensitivity and +5 dBm Maximum Input Level
- +0 dBm Typical Output Power and 38.75 dB TX Power Control Range
- Differential RF Input/Output and Integrated TX/RX Switch
- Integrated Low Phase Noise VCO, Frequency Synthesizer and PLL Loop Filter
- Digital VCO and Filter Calibration
- Integrated RSSI ADC and I/Q DACs
- Integrated LDO
- High Receiver and RSSI Dynamic Range

MAC/Baseband Features:
- Hardware CSMA-CA Mechanism, Automatic ACK Response and FCS Check
- Independent Beacon, Transmit and GTS FIFO
- Hardware Security Engine (AES-128) with CTR, CCM and CBC-MAC modes
- Supports all CCA modes and RSS/LQI
- Automatic Packet Retransmit Capability
- Supports In-Line or Stand-Alone modes for both Encryption and Decryption

Pin Diagram:

Note: Backside center pad is GND.
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1.0 OVERVIEW

The MRF24J40 is an IEEE 802.15.4-2003 compliant transceiver supporting MiWi™, ZigBee™ and other proprietary protocols. The MRF24J40 integrates wireless RF, PHY layer baseband and MAC layer architectures that can be combined with a simple microprocessor to apply low data rate to a multitude of applications that include home automation, consumer electronics, PC peripherals, toys, industrial automation and more. The MRF24J40 device integrates a receiver, transmitter, VCO and PLL into a single integrated circuit. It uses advanced radio architecture to minimize external part count and power consumption. The MRF24J40 MAC/baseband provides hardware architecture for both IEEE 802.15.4 MAC and PHY layers. It mainly consists of TX/RX FIFOs, a CSMA-CA controller, superframe constructor, receive frame filter, security engine and digital signal processing module. The MRF24J40 is fabricated by advanced 0.18 μm CMOS process and is offered in a 40-pin QFN 6x6 mm² package.

Features are summarized in Table 1-1 and the pinout for this device is listed in Table 1-2.

The MRF24J40 consists of four major functional blocks:
1. An SPI interface that serves as a communication channel between the host controller and the MRF24J40.
2. Control registers which are used to control and monitor the MRF24J40.
3. The MAC (Medium Access Control) module that implements IEEE 802.3™ compliant MAC logic.
4. The PHY (Physical Layer) driver that encodes and decodes the analog data.

The device also contains other support blocks, such as the on-chip voltage regulator, security module and system control logic.

<table>
<thead>
<tr>
<th>TABLE 1-1: DEVICE FEATURES FOR THE MRF24J40 (40-PIN DEVICE)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Features</strong></td>
</tr>
<tr>
<td>----------------</td>
</tr>
<tr>
<td>IEEE 802.15.4™ Specification Compliant</td>
</tr>
<tr>
<td>Integrated Oscillator Drive</td>
</tr>
<tr>
<td>Reference Clock Output</td>
</tr>
<tr>
<td>Power-Saving Mode Support</td>
</tr>
<tr>
<td>Current Consumption</td>
</tr>
<tr>
<td>Sleep Mode</td>
</tr>
<tr>
<td>Serial Communications</td>
</tr>
<tr>
<td>Packages</td>
</tr>
</tbody>
</table>
FIGURE 1-1: MRF24J40 ARCHITECTURE BLOCK DIAGRAM

User Application

ZigBee™ Protocol
  or
MiWi™ Protocol
  or
Proprietary Protocol

Physical Layer Driver

Interrupt

SPI Interface

Reset

TX FIFOs
Long Control Registers
Short Control Registers
RX FIFO

TX MAC
Security Module
RX MAC

TX PHY
RX PHY

MRF24J40
### 1.1 Pin Descriptions

**TABLE 1-2: MRF24J40 PIN DESCRIPTIONS**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Power</td>
<td>RF power supply. Bypass with a capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>2</td>
<td>RFP</td>
<td>AIO</td>
<td>Differential RF input/output (+).</td>
</tr>
<tr>
<td>3</td>
<td>RFN</td>
<td>AIO</td>
<td>Differential RF input/output (-).</td>
</tr>
<tr>
<td>4</td>
<td>VDD</td>
<td>Power</td>
<td>RF power supply. Bypass with a capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>5</td>
<td>VDD</td>
<td>Power</td>
<td>Guard ring power supply. Bypass with a capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>Ground</td>
<td>Guard ring ground.</td>
</tr>
<tr>
<td>7</td>
<td>GPIO0</td>
<td>DIO</td>
<td>General purpose digital I/O, also used as external PA enable.</td>
</tr>
<tr>
<td>8</td>
<td>GPIO1</td>
<td>DIO</td>
<td>General purpose digital I/O, also used as external TX/RX switch control.</td>
</tr>
<tr>
<td>9</td>
<td>GPIO5</td>
<td>DIO</td>
<td>General purpose digital I/O.</td>
</tr>
<tr>
<td>10</td>
<td>GPIO4</td>
<td>DIO</td>
<td>General purpose digital I/O.</td>
</tr>
<tr>
<td>11</td>
<td>GPIO2</td>
<td>DIO</td>
<td>General purpose digital I/O, also used as external TX/RX switch control.</td>
</tr>
<tr>
<td>12</td>
<td>GPIO3</td>
<td>DIO</td>
<td>General purpose digital I/O.</td>
</tr>
<tr>
<td>13</td>
<td>RESET</td>
<td>DI</td>
<td>Global hardware Reset pin active-low.</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>Ground</td>
<td>Ground for digital circuit.</td>
</tr>
<tr>
<td>15</td>
<td>WAKE</td>
<td>DI</td>
<td>External wake-up trigger.</td>
</tr>
<tr>
<td>16</td>
<td>INT</td>
<td>DO</td>
<td>Interrupt pin to microcontroller.</td>
</tr>
<tr>
<td>17</td>
<td>SDO</td>
<td>DIO</td>
<td>Serial interface data output from MRF24J40.</td>
</tr>
<tr>
<td>18</td>
<td>SDI</td>
<td>DIO</td>
<td>Serial interface data input to MRF24J40.</td>
</tr>
<tr>
<td>19</td>
<td>SCK</td>
<td>DI</td>
<td>Serial interface clock.</td>
</tr>
<tr>
<td>20</td>
<td>CS</td>
<td>DI</td>
<td>Serial interface enable.</td>
</tr>
<tr>
<td>21</td>
<td>VDD</td>
<td>Power</td>
<td>Digital circuit power supply. Bypass with a capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>22</td>
<td>GND</td>
<td>Ground</td>
<td>Ground for digital circuit.</td>
</tr>
<tr>
<td>23</td>
<td>NC</td>
<td>—</td>
<td>No Connection, do not connect anything to this pin.</td>
</tr>
<tr>
<td>24</td>
<td>GND</td>
<td>Ground</td>
<td>Ground for digital circuit.</td>
</tr>
<tr>
<td>25</td>
<td>GND</td>
<td>Ground</td>
<td>Ground for digital circuit.</td>
</tr>
<tr>
<td>26</td>
<td>CLKOUT</td>
<td>DIO</td>
<td>20/10/5/2.5 MHz clock output.</td>
</tr>
<tr>
<td>27</td>
<td>LPOSC2</td>
<td>AI</td>
<td>32 kHz crystal input (-).</td>
</tr>
<tr>
<td>28</td>
<td>LPOSC1</td>
<td>AI</td>
<td>32 kHz crystal input (+).</td>
</tr>
<tr>
<td>29</td>
<td>RXIP</td>
<td>AO</td>
<td>Analog RX I channel output (+).</td>
</tr>
<tr>
<td>30</td>
<td>RXQP</td>
<td>AO</td>
<td>Analog RX Q channel output (+).</td>
</tr>
<tr>
<td>31</td>
<td>VDD</td>
<td>Power</td>
<td>Power supply for band gap reference circuit. Bypass with a capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>32</td>
<td>VDD</td>
<td>Power</td>
<td>Power supply for analog circuit. Bypass with a capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>33</td>
<td>OSC2</td>
<td>AI</td>
<td>20 MHz crystal input (-).</td>
</tr>
<tr>
<td>34</td>
<td>OSC1</td>
<td>AI</td>
<td>20 MHz crystal input (+).</td>
</tr>
<tr>
<td>35</td>
<td>VDD</td>
<td>Power</td>
<td>PLL power supply. Bypass with a capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>36</td>
<td>GND</td>
<td>Ground</td>
<td>Ground for PLL.</td>
</tr>
<tr>
<td>37</td>
<td>VDD</td>
<td>Power</td>
<td>Charge pump power supply. Bypass with a capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>38</td>
<td>NC</td>
<td>—</td>
<td>No Connection.</td>
</tr>
<tr>
<td>39</td>
<td>VDD</td>
<td>Power</td>
<td>VCO supply. Bypass with a capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>40</td>
<td>LCAP</td>
<td>—</td>
<td>PLL loop filter external capacitor. Connected to external 180 pF capacitor.</td>
</tr>
</tbody>
</table>

**Legend:**  
A = Analog, D = Digital, I = Input, O = Output
## 2.0 EXTERNAL CONNECTIONS

### 2.1 Oscillator

The MRF24J40 is designed to operate at 20 MHz with a crystal connected to the OSC1 and OSC2 pins. A typical oscillator circuit is shown in Figure 2-1.

**FIGURE 2-1: CRYSTAL OSCILLATOR OPERATION**

![Crystal Oscillator Circuit](image)

**Note 1:** A series resistor (Rs) may be required for AT strip cut crystals.

### 2.2 Oscillator Start-up

The MRF24J40 PHY has an internal PLL that must lock before the device is capable of transmitting or receiving packets. After a full Power-on Reset, the device requires 2 ms to lock. During this delay, all registers and buffer memory may still be read and written to through the SPI bus. However, software should not attempt to transmit any packets (set the TXRTS (TXNMTRIG<0>)), or access any MAC or PHY registers during this period.

### 2.3 CLKOUT Pin

The clock out pin is provided to the system designer for use as the host controller clock or as a clock source for other devices in the system. The CLKOUT has an internal prescaler which can divide the output by 1, 2, 4 or 8. The CLKOUT function is enabled via the CLKCTRL register (Register 2-1) and the prescaler is selected via the RFCTRL7 register (Register 2-2).

### REGISTER 2-1: CLKCTRL: DIVIDED SLEEP CLOCK (50 kHz) SELECTION REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>r</td>
<td>—</td>
<td>CLKOEN</td>
<td>SCLKDIV&lt;4:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- **1** = Bit is set
- **0** = Bit is cleared
- **x** = Bit is unknown

- **bit 7** = Reserved: Maintain as ‘0’
- **bit 6** = Unimplemented: Read as ‘0’
- **bit 5** = CLKOEN: 20 MHz Clock Output Enable bit
  - 1 = Disable
  - 0 = Enable
- **bit 4-0** = SCLKDIV4:SCLKDIV0: Divided SLPCLK Selection bits
  - Divided by $2^n$. 

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To create a clean clock signal, the CLKOUT pin is held low for a period when power is first applied. After the Power-on Reset ends, the Oscillator Start-up Timer (OST) will begin counting. When the OST expires, the CLKOUT pin will begin outputting its default frequency of 2.5 MHz (main clock divided by 8).

### REGISTER 2-2: RFCTRL7: RF CONTROL REGISTER 7

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SLPCLK&lt;7:6&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CLKDIV&lt;1:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ’1’ = Bit is set
- ’0’ = Bit is cleared
- x = Bit is unknown

**bit 7-6**  **SLPCLK7:SLPCLK6:** Sleep Clock Selection bits
- 00 = None
- 01 = External crystal
- 10 = Internal ring oscillator
- 11 = Reserved

**bit 5-2**  **Unimplemented:** Read as ‘0’

**bit 1-0**  **CLKDIV1:CLKDIV0:** MRF24J40 Clock Output Frequency bits
- 00 = 2.5 MHz
- 01 = 5 MHz
- 10 = 10 MHz
- 11 = 20 MHz

### 2.4 RF Output

RFP and RFN are the differential RF input/output pins. These pins are connected to the antenna of the system, as seen in the example circuit diagram in Figure A-1. L5 is an RF choke. This inductor filters out non 2.4 GHz voltages. L3, L4, C37 and C43 act as a balun. The balun converts a differential unbalanced input and converts it to a balanced singled-ended output and visa versa. L1, C23 and C38 form a pi-type matching circuit to match the impedance of the balun to the impedance of the antenna. This circuit is not required if the impedance of the balun matches the antenna impedance. Refer to Appendix A.1 “Layout Considerations and RF Measurements” for more details about board layout and part selection concerning the RF output pins.
3.0 MEMORY ORGANIZATION

All memory in the MRF24J40 is implemented as static RAM. There are five types of memory in the MRF24J40:

- Short Address Control Registers
- Long Address Control Registers
- Transmit Buffers
- Receive Buffers
- Security Buffer

The control registers, both long and short, are used for configuration, control, and status retrieval of the MRF24J40. The control registers are directly read and written to by the SPI interface. The transmit and receive buffers contain transmit and receive memory used by the controller to transmit and receive data.

The security buffer provides an engine for the MRF24J40 MAC, which is compatible with the IEEE 802.15.4 LR-WPAN (ZigBee). The security buffer contains the following features:

- Transmit encryption and receive decryption.
- Seven-mode security suite.
- 64 x 8-bit security RAM for security suite storing: one receive key and three transmit keys for TX FIFOs. Beacon FIFO and GTS2 FIFO share the same key space since they will not conflict with each other. Normal FIFO and GTS1 FIFO both have their own transmit key.
- Security of APL and NWK layers can be achieved using the same engine. The upper layer security function is compliant to the ZigBee V1.0 and ZigBee 2006 specifications.

The SPI interface used to write and read these registers is described in Section 4.0 “Serial Peripheral Interface (SPI)”.

Figure 3-1 shows the data memory organization for the MRF24J40.
3.1 Control Registers

The control registers provide the main interface between the host controller and the on-chip RF controller logic. Writing to these registers controls the operation of the interface, while reading the registers allows the host controller to monitor operations.

The control register memory is partitioned into the short address control register section and the long address control register section.

All reserved registers may be read but their contents must not be changed. When reading and writing to registers which contain reserved bits, any rules stated in the register definition should be observed.

**FIGURE 3-2: MRF24J40 SHORT ADDRESS CONTROL REGISTER MAPPING**

| 00h RXMCR | 10h — | 20h — | 30h — |
| 01h PANIDL | 11h — | 21h — | 31h ISRSTS |
| 02h PANIDH | 12h — | 22h — | 32h INTMSK |
| 03h SADR0 | 13h — | 23h — | 33h GPIO |
| 04h SADR1 | 14h — | 24h TXSR |
| 05h SADR2 | 15h — | 25h — |
| 06h SADR3 | 16h — | 26h — |
| 07h SADR4 | 17h — | 27h — |
| 08h SADR5 | 18h — | 28h — |
| 09h SADR6 | 19h — | 29h — |
| 0Ah SADR7 | 1Ah — | 2Ah — |
| 0Bh SADR8 | 1Bh — | 2Bh — |
| 0Ch RXFLUSH | 1Ch — | 2Ch — |
| 0Dh — | 1Dh — | 2Dh — |
| 0Eh — | 1Eh — | 2Eh — |
| 0Fh — | 1Fh — | 2Fh — |

**FIGURE 3-3: MRF24J40 LONG ADDRESS CONTROL REGISTER MAPPING**

| 200h RFCTRL0 | 210h — | 220h CLKCTRL | 230h — | 240h — |
| 201h — | 211h — | 221h — | 231h — | 241h — |
| 202h RFCTRL1 | 212h — | 222h — | 232h — | 242h — |
| 203h RFCTRL2 | 213h — | 223h — | 233h — | 243h — |
| 204h — | 214h — | 224h — | 234h — | 244h — |
| 205h — | 215h — | 225h — | 235h — | 245h — |
| 206h RFCTRL3 | 216h — | 226h — | 236h — | 246h — |
| 207h RFCTRL4 | 217h — | 227h — | 237h — | 247h — |
| 208h RFCTRL5 | 218h — | 228h — | 238h — | 248h — |
| 209h — | 219h — | 229h — | 239h — | 249h — |
| 20Ah — | 21Ah — | 22Ah — | 23Ah — | 24Ah — |
| 20Bh — | 21Bh — | 22Bh — | 23Bh — | 24Bh — |
| 20Ch — | 21Ch — | 22Ch — | 23Ch — | 24Ch — |
| 20Dh — | 21Dh — | 22Dh — | 23Dh — | 24Dh — |
| 20 Eh — | 21 Eh — | 22 Eh — | 23 Eh — | 24 Eh — |
| 20Fh — | 21Fh — | 22Fh — | 23Fh — | 24Fh — |
## 3.2 MRF24J40 Address Summary

### TABLE 3-1: REGISTER FILE SHORT ADDRESS SUMMARY

<table>
<thead>
<tr>
<th>File Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR</th>
<th>Details on page:</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXMCR</td>
<td>TXCRCN</td>
<td>BBLPBK</td>
<td>ACKEN</td>
<td>MACLPBK</td>
<td>PANCOORD</td>
<td>COORD</td>
<td>RXCRCEN</td>
<td>PROMI</td>
<td>0000 0000</td>
<td>21</td>
</tr>
<tr>
<td>PANIDL</td>
<td>MAC PAN Low Byte (PANL&lt;7:0&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PANIDH</td>
<td>MAC PAN High Byte (PANH&lt;15:8&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SADDRL</td>
<td>MAC Short Address Low Byte (SADDRL&lt;7:0&gt;)</td>
<td>0000 0000</td>
<td>27</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SADDRH</td>
<td>MAC Short Address High Byte (SADDRH&lt;15:8&gt;)</td>
<td>0000 0000</td>
<td>27</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EADR0</td>
<td>LSB of EU (EADR0&lt;7:0&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EADR1</td>
<td>Byte 2 of EU (EADR1&lt;15:8&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EADR2</td>
<td>Byte 3 of EU (EADR2&lt;23:16&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EADR3</td>
<td>Byte 4 of EU (EADR3&lt;31:24&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EADR4</td>
<td>Byte 5 of EU (EADR4&lt;39:32&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EADR5</td>
<td>Byte 6 of EU (EADR5&lt;47:40&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EADR6</td>
<td>Byte 7 of EU (EADR6&lt;55:48&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EADR7</td>
<td>MSB of EU (EADR7&lt;63:56&gt;)</td>
<td>0000 0000</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXFLUSH</td>
<td>—</td>
<td>r</td>
<td>r</td>
<td>RXWRTBLK</td>
<td>CMDONLY</td>
<td>DATAONLY</td>
<td>BCNONLY</td>
<td>RXFLUSH</td>
<td>-000 0000</td>
<td>34</td>
</tr>
<tr>
<td>TXNMTRIG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>TXS</td>
<td>TXRETRY&lt;7:6&gt;</td>
<td>CCAFAIL</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>0000 0000</td>
<td>31</td>
</tr>
<tr>
<td>ISRSTS</td>
<td>SLPF</td>
<td>WAKEF</td>
<td>HSYMTRIF</td>
<td>SECIF</td>
<td>RXIF</td>
<td>GTS2TXIF</td>
<td>GTS1TXIF</td>
<td>TXIF</td>
<td>0000 0000</td>
<td>36</td>
</tr>
<tr>
<td>INTMSK</td>
<td>SLPSK</td>
<td>WAKMSK</td>
<td>HSYMTRIFMSK</td>
<td>SECMSK</td>
<td>RXMSK</td>
<td>GTS2TXMSK</td>
<td>GTS1TXMSK</td>
<td>TXMSK</td>
<td>1111 1111</td>
<td>37</td>
</tr>
<tr>
<td>GPIO</td>
<td>—</td>
<td>—</td>
<td>GPIO5</td>
<td>GPIO4</td>
<td>GPIO3</td>
<td>GPIO2</td>
<td>GPIO1</td>
<td>GPIO0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>TRISGP0</td>
<td>—</td>
<td>—</td>
<td>TRISGP5</td>
<td>TRISGP4</td>
<td>TRISGP3</td>
<td>TRISGP2</td>
<td>TRISGP1</td>
<td>TRISGP0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>RFCCTL</td>
<td>r</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>BBREG2</td>
<td>CCCAMODE&lt;7:6&gt;</td>
<td>CCATHRES&lt;5:2&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0000 0000</td>
<td>25</td>
</tr>
<tr>
<td>BBREG6</td>
<td>RSSIREQ</td>
<td>RXRSSI</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>RSSIRDY</td>
<td>0000 0001</td>
</tr>
<tr>
<td>RSSIITHCCA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:**
- = unimplemented, r = reserved. Shaded cells are unimplemented, read as '0'.

### TABLE 3-2: REGISTER FILE LONG ADDRESS SUMMARY

<table>
<thead>
<tr>
<th>File Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR</th>
<th>Details on page:</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFCTRL0</td>
<td>CHANNEL&lt;7:4&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0000 0000</td>
<td>24</td>
</tr>
<tr>
<td>RFCTRL2</td>
<td>RFPLL</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0000 0000</td>
<td>22</td>
</tr>
<tr>
<td>RFCTRL3</td>
<td>TXPOWER&lt;7:3&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0000 0000</td>
<td>22</td>
</tr>
<tr>
<td>RFCTRL6</td>
<td>TXFIL</td>
<td>—</td>
<td>r</td>
<td>r</td>
<td>BATMONEN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0000 0000</td>
<td>23</td>
</tr>
<tr>
<td>RFCTRL7</td>
<td>SLPCLK&lt;7:8&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0000 0000</td>
<td>23</td>
</tr>
<tr>
<td>RFCTRL8</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RF_VCO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>23</td>
</tr>
<tr>
<td>CLKINTCR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>CLKCTRL1</td>
<td>r</td>
<td>—</td>
<td>—</td>
<td>CLKEN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:**
- = unimplemented, r = reserved. Shaded cells are unimplemented, read as '0'.

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4.0 SERIAL PERIPHERAL INTERFACE (SPI)

4.1 Overview
The MRF24J40 is designed to interface directly with the Serial Peripheral Interface (SPI) port available on many microcontrollers. The implementation used on this device supports SPI mode 0,0 only. In addition, the SPI port requires that SCK be Idle in a low state; selectable clock polarity is not supported.

Commands and data are sent to the device via the SDI pin, with data being clocked in on the rising edge of SCK. Data is driven out by the MRF24J40 on the SDO line, on the falling edge of SCK. The CS pin must be held low while any operation is performed and returned high when finished.

The MRF24J40 accesses the short and long RAM banks in a slightly different manner. The following sections describe the required waveforms in order to read and write from both short and long RAM addresses.

FIGURE 4-1: SPI INPUT TIMING

FIGURE 4-2: SPI OUTPUT TIMING
4.2 Short Address Register Interface

4.2.1 READING SHORT ADDRESS REGISTERS

The short address space is accessed by sending a ‘0’ as the first bit of the SPI transfer. The following 6 bits are the address of the target register. The final bit of the first byte is a '0' to indicate that the command is a read. On the next clock edge of SCK, the Most Significant bit of the register will shift out, followed by the rest of the bits.

FIGURE 4-3: SHORT ADDRESS READ

EXAMPLE 4-1: SHORT ADDRESS READ EXAMPLE

```c
BYTE GetShortRAMAddress(BYTE address)
{
    BYTE toReturn;
    CSn = 0;
    SPIPut((address<<1)&0b01111110);
    toReturn = SPIGet();
    CSn = 1;
    return toReturn;
}
```
4.2.2 WRITING SHORT ADDRESS
REGISTERS

The short address space is accessed by sending a ‘0’ as the first bit of the SPI transfer. The following 6 bits are the address of the target register. The final bit of the first byte is a ‘1’ to indicate that the command is a write. On the next clock edge of SCK, the Most Significant bit of the register will shift out, followed by the rest of the bits.

**FIGURE 4-4: SHORT ADDRESS WRITE**

**EXAMPLE 4-2: SHORT ADDRESS WRITE EXAMPLE**

```c
void SetShortRAMAddress(BYTE address, BYTE value) {
    CSn = 0;
    SPIPut(((address<<1)&0b01111111)|0x01);
    SPIPut(value);
    SPIPut(0x01);
    CSn = 1;
}
```
4.3 Long Address Register Interface

4.3.1 READING LONG ADDRESS REGISTERS

The long address space is accessed by sending a ‘1’ as the first bit of the SPI transfer. The following 10 bits are the address of the target register. The final bit is a ‘0’ to indicate that the command is a read. On the next clock edge of SCK, the Most Significant bit of the register will shift out, followed by the rest of the bits.

FIGURE 4-5: LONG ADDRESS READ

EXAMPLE 4-3: LONG ADDRESS READ EXAMPLE

```c
BYTE GetLongRAMAddress(WORD address)
{
    BYTE toReturn;
    CSn = 0;
    SPIPut(((address>>3)&0b01111111)|0x80);
    SPIPut(((address<<5)&0b11100000));
    toReturn = SPIGet();
    CSn = 1;
    return toReturn;
}
```
4.3.2 WRITING LONG ADDRESS REGISTERS

The long address space is accessed by sending a ‘1’ as the first bit of the SPI transfer. The following 10 bits are the address of the target register. The final bit is a ‘1’ to indicate that the command is a write. On the next clock edge of SCK, the Most Significant bit of the register will shift out, followed by the rest of the bits.

4.4 Buffer Interface

The receive and transmit buffers in the MRF24J40 are located in the long RAM address space. These buffers are accessed using the same process as accessing the long RAM control addresses. The received buffer is read-only and should not be written to. The use of these buffers is described in Section 7.0 “Transmitting and Receiving Packets”.

FIGURE 4-6: LONG ADDRESS WRITE

EXAMPLE 4-4: LONG ADDRESS WRITE EXAMPLE

```c
void SetLongRAMAddress(WORD address, BYTE value)
{
    CSn = 0;
    SPIPut(((BYTE)(address>>3))&0b01111111)|0x80);
    SPIPut(((BYTE)(address<<5))&0b11100000)|0x10);
    SPIPut(value);
    CSn = 1;
}
```
5.0 IEEE 802.15.4™-2003

5.1 Overview

Before discussing the use of the MRF24J40, it may be helpful to review the structure of a typical data frame. Users requiring more information should refer to the IEEE 802.15.4 Standard.

5.2 Packet Format

Normal IEEE 802.15.4 compliant packets are between 5 and 127 bytes long. They are made up of several possible fields: destination address information, source address information, a length field, data payload and a Cyclic Redundancy Check (CRC). Additionally, a 4-byte preamble field and Start-of-Frame Delimiter (SFD) byte are appended to the beginning of the packet. Thus, traffic seen on the air will appear as shown in Figure 5-1.

![Packet Format Diagram]

- **Number of Bytes**
  - 4: Preamble
  - 1: SFD
  - 1: Packet Length
  - 2: Frame Control
  - 1: Sequence Number
  - 0/4/10: Destination Address Information
  - 0/2/8/10: Source Address Information
  - 0-122: Data Payload
  - 2: FCS

- **Comments**
  - Filtered out by module
  - Start-of-Frame delimiter – Filtered out by module
  - Used to calculate FCS
  - Used to calculate packet length
  - Short or long address of the destination device plus the PAN identifier. Length selected in the frame control.
  - Short or long address of the source device plus the PAN identifier. Length selected in the frame control.
  - Frame check sequence – CRC
5.2.1 PREAMBLE/START-OF-FRAME DELIMITER
When transmitting and receiving data with the MRF24J40, the preamble and Start-of-Frame delimiter bytes will automatically be generated or stripped from the packets when they are transmitted or received. The host controller does not need to concern itself with them. Normally, the host controller will also not need to concern itself with the CRC, which the MRF24J40 will also be able to automatically generate when transmitting and verify when receiving. The CRC fields will, however, be written into the receive buffer when packets arrive, so they may be evaluated by the host controller if needed.

5.2.2 LENGTH
The length field is a 1-byte field which defines the size of the packet excluding itself, the preamble and SFD, but including all other bytes of the packet, including FCS.

5.2.3 FRAME CONTROL
The frame control field describes the format of this packet. It defines the type of packet (beacon, data, ACK, etc.), the addressing modes used, if the packet is encrypted or not, if the packet requires an ACK, and if the packet is an intra-PAN network. This information is used by the host controller to determine how to decipher the data that follows the frame control field.

5.2.4 SEQUENCE NUMBER
The sequence number field is a 1-byte sequence number that distinguishes packets. The sequence number field is used in the Acknowledgement process. An ACK packet contains no addressing information, so the uniqueness of the sequence number is the sole determining factor for verifying that a packet reached its destination. The MRF24J40 has an Auto-Acknowledgement feature that is described in Section 7.1 “Transmitting Packets”.

5.2.5 DESTINATION ADDRESS INFORMATION
The destination address fields of an IEEE 802.15.4 packet can change depending on the frame control field of that packet. The frame control field can specify that no destination address is present, or can specify that the short address (2 bytes) or long address (8 bytes) is present. The frame control can also specify, by using the intra-PAN bit, that the source PAN matches the destination PAN and is thus, not included in the packet.

Long addresses consist of two portions. The first three bytes are known as the Extended Organizationally Unique Identifier (EUI). EUIs are distributed by the IEEE 802.15.4. The last five bytes are address bytes which can contain the needed requirements at the discretion of the company that purchased the EUI.

When transmitting packets, the assigned source long or short address, depending on the setting of the frame control field, must be written into the transmit buffer by the host controller. The MRF24J40 will not automatically include the source address information.

5.2.6 SOURCE ADDRESS INFORMATION
The source address fields of an IEEE 802.15.4 packet can change depending on the frame control field of that packet. The frame control field can specify that no destination address is present, or can specify that the short address (2 bytes) or long address (8 bytes) is present. The frame control can also specify, by using the intra-PAN bit, that the source PAN matches the destination PAN and is thus, not included in the packet.

5.2.7 DATA
The data section of the packet can vary in length from 0 bytes to 122 bytes. Packets that exceed 127 bytes, including the frame control, source addressing, destination addressing, data and FCS fields, will be filtered out by the MRF24J40.

5.2.8 FCS
The FCS field is a 2-byte field which contains an industry standard, 16-bit CRC calculated with the data from the frame control, sequence number, destination, source, and data fields. When receiving packets, the MRF24J40 will check the CRC of each incoming packet. If the RXCRCEN bit (RXMCR<7>) is cleared, packets with invalid CRCs will automatically be discarded. If RXCRCEN is set, and the packet meets all other receive filtering criteria, the packet will be written into the receive buffer and the host controller will be able to determine if the CRC was valid by reading the receive status vector (see Section 7.3 “Receiving Packets”).

When transmitting packets, the MRF24J40 will automatically generate a valid CRC and transmit it attached to the end of the packet if the TXCRCEN bit (TXMCR<7>) is cleared.
6.0 INITIALIZATION

6.1 Overview

Before the MRF24J40 can be used to transmit and receive packets, certain device settings must be initialized. Depending on the application, some configuration options may need to be changed. Normally, these tasks may be accomplished once after Reset and do not need to be changed thereafter.

6.2 Receive Filters

To minimize the processing requirements of the host controller, the MRF24J40 incorporates several different receive filters which can automatically reject packets which are not needed. These options are controlled through the RXMCR register.

REGISTER 6-1: RXMCR: RECEIVE FILTER CONTROL REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXCRCEN</td>
<td>r</td>
<td>ACKEN</td>
<td>r</td>
<td>PANCOORD</td>
<td>COORD</td>
<td>RXCRCEN</td>
<td>PROMI</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘n’ = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- **bit 7 TXCRCEN**: No CRC Data with Normal FIFO bit
  1 = CRC is disabled for the TX FIFO
  0 = CRC is enabled for the TX FIFO

- **bit 6 Reserved**: Maintain as ‘0’

- **bit 5 ACKEN**: No ACK Respond in Any Case bit
  1 = ACK response is always disabled
  0 = ACK response enabled. ACKs are returned when they are requested.

- **bit 4 Reserved**: Maintain as ‘0’

- **bit 3 PANCOORD**: PAN Coordinator bit
  1 = Set as PAN coordinator
  0 = Not set as PAN coordinator

- **bit 2 COORD**: Coordinator bit
  1 = Set as coordinator
  0 = Not set as coordinator

- **bit 1 RXCRCEN**: Error Report bit
  1 = RX all kinds of PKT (including CRC error)
  0 = Only RX PKT (CRC ok)

- **bit 0 PROMI**: RX All Kinds of PKT bit (CRC ok)
  1 = RX all kinds of PKT (CRC ok)
  0 = Discard PKT when there is a MAC address mismatch, illegal frame type, dPAN/sPAN or MAC short address mismatch
### 6.3 PHY Initialization

The physical layer of the MRF24J40 controls the current levels going to different sections of the device, as well as thresholds and controls used in packet reception and transmission. There are several registers that may require modification in order to operate in the application’s intended mode.

**Note:** The RSSI threshold defaults to ‘0’, however, it can be set to a user-defined RSSI threshold limit. Please note, any RSSI value resulting from a CCA request that is below the RSSI threshold limit will result in a failure.

#### REGISTER 6-2: RFCTRL2: RF CONTROL REGISTER 2

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFPLL(1)</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7**  
  **RFPLL:** RF-PLL Control bit(1)
  - 1 = PLL enabled
  - 0 = PLL disabled

- **bit 6-3**  
  **Reserved:** Maintain as ‘0’

- **bit 2-0**  
  **Unimplemented:** Read as ‘0’

**Note 1:** PLL must be enabled for RF reception or transmission.

#### REGISTER 6-3: RFCTRL3: RF CONTROL REGISTER 3

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXPOWER&lt;7:3&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7-3**  
  **TXPOWER7:TXPOWER3:** Small Scale Control for TX Power in dB bits
  - 00000 = 0 dB
  - 00001 = -1.25 dB
  - 00010 = -2.5 dB
  - 00011 = -3.75 dB
  - 00100 = -5 dB
  - 00101 = -6.25 dB
  - 00110 = -7.5 dB
  - 00111 = -8.75 dB
  - ...
  - 11111 = -38.75 dB

- **bit 2-0**  
  **Unimplemented:** Read as ‘0’
**REGISTER 6-4: RFCTRL6: RF CONTROL REGISTER 6**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXFIL</td>
<td>—</td>
<td>r</td>
<td>r</td>
<td>BATMONEN</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7**  
  **TXFIL:** TX Filter Control bit
  - Recommended value: ‘1’.

- **bit 6**  
  **Unimplemented:** Read as ‘0’

- **bit 5-4**  
  **Reserved:** Maintain as ‘0’

- **bit 3**  
  **BATMONEN:** Battery Monitor Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **bit 2-0**  
  **Unimplemented:** Read as ‘0’

**REGISTER 6-5: RFCTRL8: RF CONTROL REGISTER 8**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SLPCLKOUT</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7-5**  
  **Unimplemented:** Read as ‘0’

- **bit 4**  
  **RF_VCO:** VCO Control bit
  - 1 = Enhanced VCO (recommended)
  - 0 = Normal VCO

- **bit 3-1**  
  **Unimplemented:** Read as ‘0’

- **bit 0**  
  **SLPCLKOUT:** 20 MHz Reference Output Clock Source bit
  - 1 = Stabilize CLKOUT while recovering from Sleep
  - 0 = Stabilize CLKOUT after a wake from Sleep

**REGISTER 6-6: RSSITHCCA: RSSI THRESHOLD FOR CCA REGISTER**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RSSITHRES&lt;7:0&gt;</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7-0**  
  **RSSITHRES7:RSSITHRES0:** RSSI Threshold for CCA/ED Mode bits
6.4 MAC Initialization

The medium access control layer of the MRF24J40 consists of several registers that define how this device operates on an IEEE 802.15.4 network.

6.4.1 DEVICE CONFIGURATION

The RXMCR, described in Section 6.2 “Receive Filters”, should be set to the appropriate value for the intended device operation. If the device is operating as a PAN coordinator, the PANCOORD bit should be set. If the device is operating as a coordinator, then the COORD bit should be set.

6.4.2 CHANNEL SELECTION

The operational channel is selected using the RFCTRL0 register.

REGISTER 6-7: RFCTRL0: RF CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHANNEL&lt;7:4&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7—bit 0

Legend:

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’

-n = Value at POR  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

bit 7:4  
CHANNEL7:CHANNEL4: Channel Number bits

00000 = Channel 11  
00001 = Channel 12  
00010 = Channel 13  
…  
11111 = Channel 26

bit 3-0  
Unimplemented: Read as ‘0’

REGISTER 6-8: RFCTL: RF MODE CONTROL REGISTER

<table>
<thead>
<tr>
<th>W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>r</td>
<td>—</td>
<td>—</td>
<td>r</td>
<td>r</td>
<td>RFRST</td>
<td>r</td>
</tr>
</tbody>
</table>

bit 7—bit 0

Legend:

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’

-n = Value at POR  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

bit 7  
Reserved: Maintain as ‘0’

bit 6-5  
Unimplemented: Read as ‘0’

bit 4-3  
Reserved: Maintain as ‘0’

bit 2  
RFRST: RF Reset bit

1 = Reset RF (turn off RF)  
0 = Normal operation

bit 1-0  
Reserved: Maintain as ‘0’
### REGISTER 6-9: BBREG2: BASEBAND CCA/RSSI MODE REGISTER 2

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCAMODE&lt;7:6&gt;</td>
<td>CCATHRES&lt;5:2&gt;</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(x\) = Bit is unknown

**bit 7-6**

<table>
<thead>
<tr>
<th>CCAMODE7:CCAMODE6: CCA Mode bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 = Reserved</td>
</tr>
<tr>
<td>01 = CCA Mode 1, carrier sense only</td>
</tr>
<tr>
<td>10 = CCA Mode 2, energy above threshold</td>
</tr>
<tr>
<td>11 = CCA Mode 3, carrier sense with energy above threshold</td>
</tr>
</tbody>
</table>

**bit 5-2**

<table>
<thead>
<tr>
<th>CCATHRES5:CCATHRES2: CCA Carrier Sense Threshold bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCA/CS value set to 0xE or ‘1110’.</td>
</tr>
</tbody>
</table>

**bit 1-0**

| Unimplemented: Read as ‘0’ |

### REGISTER 6-10: BBREG6: BASEBAND RSSI MODE REGISTER 6

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSSIREQ</td>
<td>RXRSSI</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>RSSIRDY</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(x\) = Bit is unknown

**bit 7**

<table>
<thead>
<tr>
<th>RSSIREQ: RSSI Mode 1 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = Initiate an RSSI calculation (write back to ‘0’ when complete)</td>
</tr>
<tr>
<td>0 = Otherwise</td>
</tr>
</tbody>
</table>

**bit 6**

<table>
<thead>
<tr>
<th>RXRSSI: RSSI Mode 2 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = Calculating RSSI for RX packet</td>
</tr>
<tr>
<td>0 = No calculating RSSI for RX packet</td>
</tr>
</tbody>
</table>

**bit 5-1**

| Reserved: Maintain as ‘0’ |

**bit 0**

<table>
<thead>
<tr>
<th>RSSIRDY: RSSI Ready Signal Firmware Request bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = RSSI value ready</td>
</tr>
<tr>
<td>0 = Otherwise</td>
</tr>
</tbody>
</table>
6.4.3 LONG ADDRESSES
Every device in the world has a unique long address. Long addresses are described in more detail in Section 5.2.5 “Destination Address Information” and Section 5.2.6 “Source Address Information”. EADR0-EADR7 are eight short RAM address registers in the MRF24J40 that are used to define the device’s long address. These addresses should be loaded into the device during the device configuration. The MRF24J40 will automatically filter out any long address packets that do not match the contents of EADR0-EADR7.

6.4.4 SHORT ADDRESS AND PAN ID
The device’s short address and PAN ID are programmed into the MRF24J40 through the SADR. L, SADR. H, PANID. L and PANID. H registers. These registers are located in the short RAM address space. The MRF24J40 automatically filters out packets that are specified as short address destinations with addresses that do not match these registers. The exception to this rule is packets with the broadcast short address (FFFFh) and/or the broadcast PAN ID (FFFFh). Packets that match the short address and have the broadcast PAN ID will be accepted, as well as packets with the broadcast short address that match the PAN ID. A true broadcast packet will have both the short address and PAN ID set to the broadcast address. The MRF24J40 will also receive these packets no matter what the setting of the short address and PAN ID registers.

Example 6-1 shows how to initialize the MRF24J40.

---

**REGISTER 6-11: PANIDL: MAC PAN LOW BYTE REGISTER**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R/W</td>
<td>MAC PAN Low Byte (PANL&lt;7:0&gt;)</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>bit 0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown

bit 7-0  PAN7:PAN0: Lower Byte of PAN Address bits

**REGISTER 6-12: PANIDH: MAC PAN HIGH BYTE REGISTER**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R/W</td>
<td>MAC PAN High Byte (PANH&lt;15:8&gt;)</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>bit 0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown

bit 7-0  PANH15:PAN8: Higher Byte of PAN Address bits
REGISTER 6-13: SADRL: MAC SHORT ADDRESS LOW BYTE REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MAC Short Address Low Byte (SADDRL&lt;7:0&gt;)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown

bit 7-0  SADDRL7:SADDRL0: Lower Byte of Short Address bits

REGISTER 6-14: SADRH: MAC SHORT ADDRESS HIGH BYTE REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MAC Short Address High Byte (SADRH&lt;15:8&gt;)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown

bit 7-0  SADRH15:SADRH8: Higher Byte of Short Address bits
EXAMPLE 6-1: INITIALIZING THE MRF24J40

```c
void MRF24J40Init(void)
{
    BYTE i;
    WORD j;

    /* place the device in hardware reset */
    RESETn = 0;
    for(j=0;j<(WORD)300;j++){}

    /* remove the device from hardware reset */
    RESETn = 1;
    for(j=0;j<(WORD)300;j++){}

    /* reset the RF module */
    SetShortRAMAddr(RFCTL, 0x04);
    /* remove the RF module from reset */
    SetShortRAMAddr(RFCTL, 0x00);

    /* flush the RX fifo */
    SetShortRAMAddr(WRITE_RXFLUSH, 0x01);

    /* Program the short MAC Address, 0xffff */
    SetShortRAMAddr(SADRL, 0xFF);
    SetShortRAMAddr(SADRH, 0xFF);
    SetShortRAMAddr(PANIDL, 0xFF);
    SetShortRAMAddr(PANIDH, 0xFF);

    /* Program Long MAC Address */
    for(i=0;i<(BYTE)8;i++)
    {
        SetShortRAMAddr(EADR0+i*2, myLongAddress[i]);
    }

    /* enable the RF-PLL */
    SetLongRAMAddr(RFCTRL2, 0x80);

    /* set TX for max output power */
    SetLongRAMAddr(RFCTRL3, 0x00);

    /* enabled TX filter control */
    SetLongRAMAddr(RFCTRL6, 0x80);
    SetLongRAMAddr(RFCTRL8, 0b00010000);

    /* Program CCA mode using RSSI */
    SetShortRAMAddr(BBREG2, 0x78);

    /* Enable the packet RSSI */
    SetShortRAMAddr(BBREG6, 0x40);

    /* Program CCA, RSSI threshold values */
    SetShortRAMAddr(RSSITHCCA, 0x00);
    SetLongRAMAddr(RFCTRL0, 0x00); //channel 11
    SetLongRAMAddr(RFCTRL0, 0x00); //reset the RF module with new settings
    SetShortRAMAddr(RFCTL, 0x04);    //reset the RF module with new settings
    SetShortRAMAddr(RFCTL, 0x00);
}
```
7.0 TRANSMITTING AND RECEIVING PACKETS

7.1 Transmitting Packets

The MAC inside the MRF24J40 will automatically generate the preamble and Start-of-Frame delimiter fields when transmitting. Additionally, the MAC can generate any padding (if needed), and the CRC, if configured to do so. The host controller must generate and write all other frame fields into the buffer memory for transmission. Before transmitting packets, the MAC registers, which alter the transmission characteristics, should be initialized as documented in Section 6.0 “Initialization”.

7.2 TX FIFO Format

The TX MAC performs three major tasks conforming to IEEE 802.15.4:

- TX FIFO Control
- Automatic CSMA-CA and Timing Alignments
- Hardware Superframe Handling

For TX FIFO control function, TX MAC controls 4 FIFOs, including beacon, normal and 2 GTS FIFOs. When each FIFO is triggered, TX MAC performs a CSMA-CA algorithm, sends a packet to the Transmit Baseband (TXBB) at the right time, handles the retransmission if an ACK is required but not received and generates FCS bytes automatically.

The automatic CSMA-CA algorithm performs timing alignments, such as LIFS, SIFS and ACK turnaround time. The user can simply program parameters for the CSMA-CA algorithm. The TX MAC will perform automatically according these parameters.

For hardware superframe handling, TX MAC builds up the timing frame of a superframe. It includes CAP, CFP, INACTIVE and each time slot. TX MAC sends beacon, normal and GTS FIFOs at the right time, automatically, at each transmission. This largely reduces the complexity of the Beacon Enable mode of IEEE 802.15.4.

FIGURE 7-1: TRANSMIT PACKET LAYOUT

<table>
<thead>
<tr>
<th>Address</th>
<th>Memory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>Header Length</td>
<td>Length of the header. This field is described in more</td>
</tr>
<tr>
<td>0x001</td>
<td>Packet Length</td>
<td>detail in the security section of this document.</td>
</tr>
<tr>
<td>0x002-0x003</td>
<td>Frame Control</td>
<td>The length of the packet, not including the length or</td>
</tr>
<tr>
<td>0x004</td>
<td>Sequence Number</td>
<td>FCS.</td>
</tr>
<tr>
<td>0x005</td>
<td>Data[0]</td>
<td>The frame control field describing how this packet</td>
</tr>
<tr>
<td></td>
<td>Data[...]</td>
<td>should behave.</td>
</tr>
<tr>
<td>0x005 + (m – 1)</td>
<td>Data[m – 1]</td>
<td>The sequence number distinguishing this packet.</td>
</tr>
<tr>
<td>0x006 + m</td>
<td>FCS[0]</td>
<td>The destination and source addressing information,</td>
</tr>
<tr>
<td>0x007 + m</td>
<td>FCS[1]</td>
<td>as well as any application data.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The CRC value for the packet; written by hardware.</td>
</tr>
</tbody>
</table>
7.2.1 TRIGGER PACKET TRANSMISSION

The MRF24J40 handles the Clear Channel Assessment (CCA) and Carrier Sense Multiple Access Collision Avoidance (CSMA-CA) algorithms in hardware. The MRF24J40 also handles automatic retransmission of packets that require an ACK. If the frame control field of the packet requires an ACK, the ACKREQ bit (TXNMTRIG<2>) needs to be set before transmission. Once the TX FIFO is loaded with the data to transmit the TXRTS bit (TXNMTRIG<0>) is used to transmit the packet.

REGISTER 7-1: TXNMTRIG: TRIGGER AND SETTING FOR NORMAL FRAME (CAP) REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PENDACK</td>
<td>INDIRECT(1)</td>
<td>ACKREQ(1)</td>
<td>SECEN(1)</td>
<td>TXRTS</td>
</tr>
</tbody>
</table>

bit 7-5 Unimplemented: Read as ‘0’

bit 4 PENDACK: Data Pending Status in ACK bit
Status of the data pending bit in ACK from previous transmission. This bit is reset by hardware on the next transmission.
1 = Data pending bit was set
0 = Data pending bit was cleared

bit 3 INDIRECT: Activate Indirect Transmission bit(1)
1 = Indirect transmission enabled
0 = Indirect transmission disabled

bit 2 ACKREQ: TX Packet in TXN FIFO needs ACK Response bit(1)
1 = ACK requested
0 = No ACK requested

bit 1 SECEN: Secure Current TX Packet bit(1)
1 = Secure packet
0 = Send packet without securing it

bit 0 TXRTS: Trigger TX MAC to Send the Packet in TX FIFO bit
1 = Send the packet in the TX FIFO, automatically cleared by hardware

Note 1: This bit is cleared at the next triggering of TXN FIFO.
7.2.2 TRANSMISSION STATUS

When a transmission completes, the TXIF flag of the ISRSTS register will become set. Once the TXIF bit is set, the status of the transmission is located in the TXSR register.

REGISTER 7-2: TXSR: TX MAC STATUS REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>TXRETRY&lt;7:6&gt;</th>
<th>CCAFAIL</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7-6**: TXRETRY7:TXRETRY6: Retry Times bits
  Defines the retry times of the most recent TXN FIFO transmission.

- **bit 5**: CCAFAIL: Clear Channel Assessment (CCA) Status of Last Transmission bit
  - 1 = CCA failed
  - 0 = CCA passed

- **bit 4-0**: Reserved: Maintain as ‘0’

7.3 Receiving Packets

The following section details the reception of a non-secured frame. When the MRF24J40 receives a packet that passes the MAC layer addressing, threshold and packet type filters, it will indicate the reception of this packet to the host controller by setting the RXIF bit (ISRSTS<3>). The packet will remain in the buffer until the host frees the buffer. No other packets can be received while the buffer is holding a packet.

7.4 RX MAC

The RX MAC block will do CRC checking, parse the received frame type and address recognition, then store the received frame into RX FIFO. In addition to the IEEE 802.15.4 packet, there are also 2 bytes of information that are appended to the end of the packet after the FCS field: LQI and RSSI.

The behavior of RX FIFO follows a certain rule. When a received packet is not filtered or dropped, a received interrupt/status will be issued. The interrupt is read-to-clear to save host operation time. However, the RX FIFO is flushed only using the following three methods:
- The host reads the first byte and the last byte to the packet
- The host issues RX flush
- A software is reset

For RX filter function, the Promiscuous mode is supported to receive all FCS-ok packets. An Error mode is supported to receive all packets that successfully correlated PHY level preamble and delimiter.
FIGURE 7-2: RECEIVE PROCESS
7.4.1 RECEIVE PACKET LAYOUT

When a packet passes all of the enabled filters, it is placed in the receive FIFO in the following format.

**FIGURE 7-3: RECEIVE PACKET LAYOUT.**

<table>
<thead>
<tr>
<th>Address</th>
<th>Memory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x030</td>
<td>Packet Length</td>
<td>The length of the packet, not including the packet length, but does include the FCS.</td>
</tr>
<tr>
<td>0x030-0x032</td>
<td>Frame Control</td>
<td>The frame control field describing how this packet should behave.</td>
</tr>
<tr>
<td>0x033</td>
<td>Sequence Number</td>
<td>The sequence number distinguishing this packet.</td>
</tr>
<tr>
<td>0x034</td>
<td>Data[0]</td>
<td>The destination and source addressing information as well as any application data.</td>
</tr>
<tr>
<td>0x034 + (m – 1)</td>
<td>Data[m – 1]</td>
<td></td>
</tr>
<tr>
<td>0x035 + m</td>
<td>FCS[0]</td>
<td>The CRC value for the packet; written by hardware.</td>
</tr>
<tr>
<td>0x036 + m</td>
<td>FCS[1]</td>
<td></td>
</tr>
<tr>
<td>0x037 + m</td>
<td>LQI</td>
<td>The link quality index of the received packet.</td>
</tr>
<tr>
<td>0x038 + m</td>
<td>RSSI</td>
<td>The received signal strength indicator for the received packet.</td>
</tr>
</tbody>
</table>
7.4.2 FREEING RECEIVE BUFFER SPACE

The RX buffer is cleared when the length byte of the packet and the last byte of the FCS are read. Once both of these values are read from the RX buffer, the buffer will enable itself to receive another packet. Because the LQI and RSSI values are appended to the end of the packet after the FCS, it may be advisable to read these values out of the RX buffer before reading the FCS.

Alternatively, it is possible to clear the RX buffer by flushing it. This is done through the RXFLUSH register.

REGISTER 7-3: RXFLUSH: RECEIVE FIFO FLUSH REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>RXWRFTBLK</td>
<td>CMDONLY</td>
<td>DATAONLY</td>
<td>BCNONLY</td>
<td>RXFLUSH</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 7 Unimplemented: Read as ‘0’
bit 6-5 Reserved: Maintain as ‘0’
bit 4 RXWRFTBLK: Software Write to RX FIFO Address bit
1 = Writing to any RX FIFO address is enabled
0 = Writing to any RX FIFO address is disabled
bit 3 CMDONLY: Command Packet Receive bit
1 = Only command packets are received, all other packets are filtered out
0 = All valid packets are received
bit 2 DATAONLY: Data Packet Receive bit
1 = Only data packets are received, all other packets are filtered out
0 = All valid packets are received
bit 1 BCNONLY: Beacon Packet Receive bit
1 = Only beacon packets are received, all other packets are filtered out
0 = All valid packets are received
bit 0 RXFLUSH: Flush RX FIFO Address bit
1 = Flush the RX FIFO. Cleared by hardware.
0 = Previous flush complete

7.5 Transceiver

The MRF24J40 receiver features a low IF architecture and consists of an LNA, a pair of down conversion mixers, polyphase channel filters, baseband limiter amplifiers and RSSI technology. An ADC is used to sample the RSSI value and the sampled data is stored in a register from which the data can be read out via the SPI bus. The local oscillator generation circuits (VCO, PLL and buffers) are shared with the receiver and transmitter. The Low Noise Amplifier (LNA) features a differential input for high performance. The RX/TX switch is integrated and LNA input and Power Amplifier (PA) output share the same pins. A common external matching network and single-ended to differential conversion is required. The transmitter features a direct conversion architecture and has a 0 to -38.75 dBm output power. The output power adjustment is in 1.25 dB step. The TX gain is programmed by the SPI bus.
8.0 INTERRUPTS

The MRF24J40 has a simple interrupt structure. There is one interrupt pin that signals all of the possible events. The ISRSTS register is a read-to-clear register that specifies which interrupt(s) caused the interrupt. The INTMSK register is used to block unwanted interrupt sources from generating interrupts. The INTEDGE bit (CLKINTCR<1>) controls the polarity of the interrupt pin. Once ISRSTS is read by the host controller, the interrupt flags are cleared. The host controller should make certain to handle all returned flags each time the ISRSTS register is read.

8.1 Interrupt Structure

When an enabled interrupt occurs, the interrupt pin will remain at its interrupt state, as determined by the INTEDGE bit, until all of the flags which are causing the interrupt are cleared or masked off (the mask bits are set) by the host controller. If more than one interrupt source is enabled, the host controller must poll each flag in the ISRSTS register to determine the source(s) of the interrupt.

FIGURE 8-1: MRF24J40 INTERRUPT LOGIC
8.1.1 INT INTERRUPT STATUS
REGISTERS

The registers associated with the INT interrupts are shown in Register 8-1, Register 8-2 and Register 8-3.

**REGISTER 8-1: ISRSTS: INTERRUPT STATUS REGISTER**

<table>
<thead>
<tr>
<th>RC-0</th>
<th>RC-0</th>
<th>RC-0</th>
<th>RC-0</th>
<th>RC-0</th>
<th>RC-0</th>
<th>RC-0</th>
<th>RC-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLPIF</td>
<td>WAKEIF</td>
<td>HSYMTMRIF</td>
<td>SECIF</td>
<td>RXIF</td>
<td>GTS2TXIF</td>
<td>GTS1TXIF</td>
<td>TXIF</td>
</tr>
</tbody>
</table>

Legend:

<table>
<thead>
<tr>
<th>RC = Read to clear</th>
<th>W = Writable bit</th>
<th>U = Unimplemented bit, read as ‘0’</th>
</tr>
</thead>
<tbody>
<tr>
<td>-n = Value at POR</td>
<td>‘1’ = Bit is set</td>
<td>‘0’ = Bit is cleared x = Bit is unknown</td>
</tr>
</tbody>
</table>

- bit 7 **SLPIF**: Sleep Alert Interrupt bit
  - 1 = Sleep alert interrupt occurred
  - 0 = Otherwise
- bit 6 **WAKEIF**: Wake-up Alert Interrupt bit
  - 1 = Wake-up interrupt occurred
  - 0 = Otherwise
- bit 5 **HSYMTMRIF**: Half Symbol Timer Interrupt bit
  - 1 = Half symbol timer interrupt occurred
  - 0 = Otherwise
- bit 4 **SECIF**: Security Key Request Interrupt bit
  - 1 = Security key request interrupt occurred
  - 0 = Otherwise
- bit 3 **RXIF**: RX OK Interrupt bit
  - 1 = RX OK interrupt occurred
  - 0 = Otherwise
- bit 2 **GTS2TXIF**: GTS FIFO 2 Release Interrupt bit
  - 1 = GTS2 transmission interrupt occurred
  - 0 = Otherwise
- bit 1 **GTS1TXIF**: GTS FIFO 1 Release Interrupt bit
  - 1 = GTS1 transmission interrupt occurred
  - 0 = Otherwise
- bit 0 **TXIF**: TX FIFO Release Interrupt bit
  - 1 = TX FIFO transmission interrupt occurred
  - 0 = Otherwise
## REGISTER 8-2: INTMSK: INTERRUPT MASK REGISTER

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLPMSK</td>
<td>WAKEMSK</td>
<td>HSYMTMRMSK</td>
<td>SECMSK</td>
<td>RXMSK</td>
<td>GTS2TXMSK</td>
<td>GTS1TXMSK</td>
<td>TXMSK</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR
- ’1’ = Bit is set
- ’0’ = Bit is cleared
- \(x\) = Bit is unknown

**bit 7**
- **SLPMSK**: Sleep Alert Mask bit
  - 0 = Enable Sleep interrupt
  - 1 = Otherwise

**bit 6**
- **WAKEMSK**: Wake-up Alert Mask bit
  - 0 = Enable Wake interrupt
  - 1 = Otherwise

**bit 5**
- **HSYMTMRMSK**: Half Symbol Timer Mask bit
  - 0 = Enable half symbol timer interrupt
  - 1 = Otherwise

**bit 4**
- **SECMSK**: Security Interrupt Mask bit
  - 0 = Enable security interrupt
  - 1 = Otherwise

**bit 3**
- **RXMSK**: RX OK Mask bit
  - 0 = Enable receive interrupt
  - 1 = Otherwise

**bit 2**
- **GTS2TXMSK**: GTS FIFO 2 IRQ Mask bit
  - 0 = Enable GTS FIFO 2 transmit interrupt
  - 1 = Otherwise

**bit 1**
- **GTS1TXMSK**: GTS FIFO 1 IRQ Mask bit
  - 0 = Enable GTS FIFO 1 transmit interrupt
  - 1 = Otherwise

**bit 0**
- **TXMSK**: TX Normal FIFO IRQ Mask bit
  - 0 = Enable normal FIFO transmit interrupt
  - 1 = Otherwise
REGISTER 8-3:  CLKINTCR: SLPCLK ON/OFF AND INTERRUPT POLARITY REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

- bit 7-2: Unimplemented: Read as ‘0’

- bit 1: INTEDGE: Interrupt Edge Polarity bit
  
  1 = Rising edge
  
  0 = Falling edge

- bit 0: SLPCLKEN: Sleep Clock Enable bit
  
  1 = Disabled
  
  0 = Enabled
9.0 GENERAL PURPOSE I/O

9.1 GPIO Registers

The MRF24J40 has 6 available, general purpose I/O pins. These pins are interfaced through the GPIO and TRISGPIO registers.

**EXAMPLE 9-1: READ/WRITE EXAMPLE**

```c
SetShortAddress(TRISGPIO,0x03);  //set GPIO5-2 to output, and GPIO 1-0 as input
SetShortAddress(GPIO,0x01);       //set GPIO0 high and GPIO1 low.
```

**REGISTER 9-1: GPIO: GPIO PORT REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>GPIO5</td>
<td>GPIO4</td>
<td>GPIO3</td>
<td>GPIO2</td>
<td>GPIO1</td>
<td>GPIO0</td>
</tr>
</tbody>
</table>

| bit 7-6 | Unimplemented: Read as ‘0’ |
| bit 5   | GPIO5: General Purpose I/O GPIO5 bit |
| bit 4   | GPIO4: General Purpose I/O GPIO4 bit |
| bit 3   | GPIO3: General Purpose I/O GPIO3 bit |
| bit 2   | GPIO2: General Purpose I/O GPIO2 bit |
| bit 1   | GPIO1: General Purpose I/O GPIO1 bit |
| bit 0   | GPIO0: General Purpose I/O GPIO0 bit |

**Legend:**
- R =Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown
## REGISTER 9-2: TRISGPIO: GPIO PIN DIRECTION AND SPI MODE REGISTER

| bit 7-6 | Unimplemented: Read as ‘0’ |
| bit 5 | TRISGP5: General Purpose I/O GPIO5 Direction bit |
|       | 1 = Output |
|       | 0 = Input |
| bit 4 | TRISGP4: General Purpose I/O GPIO4 Direction bit |
|       | 1 = Output |
|       | 0 = Input |
| bit 3 | TRISGP3: General Purpose I/O GPIO3 Direction bit |
|       | 1 = Output |
|       | 0 = Input |
| bit 2 | TRISGP2: General Purpose I/O GPIO2 Direction bit |
|       | 1 = Output |
|       | 0 = Input |
| bit 1 | TRISGP1: General Purpose I/O GPIO1 Direction bit |
|       | 1 = Output |
|       | 0 = Input |
| bit 0 | TRISGP0: General Purpose I/O GPIO0 Direction bit |
|       | 1 = Output |
|       | 0 = Input |

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown
10.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Ambient temperature under bias.............................................................................................................. -40°C to +85°C
Storage temperature .................................................................................................................................... -65°C to +150°C
Voltage on any combined digital and analog pin with respect to VSS (except VDD)........................ -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS ............................................................................................................  -0.3V to 3.6V
Total power dissipation (Note 1) ................................................................................................................ 1.0W
Maximum output current sunk by GPIO1-GPIO5 pins ................................................................................. 1 mA
Maximum output current sourced by GPIO1-GPIO5 pins ............................................................................ 1 mA
Maximum output current sunk by GPIO0 pin .................................................................................................. 4 mA
Maximum output current sourced by GPIO0 pin .......................................................................................... 4 mA

Note 1: Power dissipation is calculated as follows:
\[ P_{\text{dis}} = V_{\text{DD}} \times (I_{\text{DD}} - \sum I_{\text{OH}}) + \sum (V_{\text{DD}} - V_{\text{OH}}) \times I_{\text{OH}} + \sum (V_{\text{OL}} \times I_{\text{OL}}) \]

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
### TABLE 10-1: RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40</td>
<td>—</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>Supply Voltage for RF, Analog and Digital Circuits</td>
<td>2.4</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage for Digital I/O</td>
<td>2.4</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Input High Voltage (VIH)</td>
<td>0.5 x VDD</td>
<td>—</td>
<td>VDD + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Input Low Voltage (VIL)</td>
<td>-0.3</td>
<td>—</td>
<td>0.2 x VDD</td>
<td>V</td>
</tr>
</tbody>
</table>

### TABLE 10-2: CURRENT CONSUMPTION

Typical Values: TA = 25°C, VDD = 3.3V

<table>
<thead>
<tr>
<th>Chip Mode</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep</td>
<td></td>
<td>2</td>
<td>TBD</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>TX</td>
<td>At maximum output power</td>
<td>22</td>
<td>TBD</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>RX</td>
<td></td>
<td>18</td>
<td>TBD</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**Legend:** TBD = To Be Determined

### TABLE 10-3: RECEIVER AC CHARACTERISTICS

Typical Values: TA = 25°C, VDD = 3.3V, LO Frequency = 2.445 GHz

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Input Frequency</td>
<td>At antenna input with O-QPSK signal and 3.5 dB front end loss is assumed</td>
<td>2.4</td>
<td>—</td>
<td>2.483</td>
<td>GHz</td>
</tr>
<tr>
<td>RF Sensitivity</td>
<td></td>
<td>—</td>
<td>-91</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Maximum RF Input</td>
<td>LNA at high gain</td>
<td>+5</td>
<td>—</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>LO Leakage</td>
<td>Measured at balun matching network input at frequency 2.405-2.48 GHz</td>
<td>—</td>
<td>-60</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>Externally matched to 50 source by a balun matching network</td>
<td>-12</td>
<td>-20</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure (including matching)</td>
<td></td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Adjacent Channel Rejection @ +/- 5 MHz</td>
<td></td>
<td>30</td>
<td>—</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Alternate Channel Rejection @ +/- 10 MHz</td>
<td></td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>RSSI Range</td>
<td></td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>RSSI Error</td>
<td></td>
<td>-5</td>
<td>—</td>
<td>5</td>
<td>dB</td>
</tr>
</tbody>
</table>
TABLE 10-4: TRANSMITTER AC CHARACTERISTICS
Typical Values: $T_a = 25^\circ C$, $V_{DD} = 3.3V$, LO Frequency = 2.445 GHz

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Carrier Frequency</td>
<td></td>
<td>2.4</td>
<td>2.483</td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>Maximum RF Output Power</td>
<td></td>
<td>0</td>
<td>0</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>RF Output Power Control Range</td>
<td></td>
<td>38.75</td>
<td>38.75</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>TX Gain Control Resolution</td>
<td>Programmed by register</td>
<td>—</td>
<td>1.25</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Carrier Suppression</td>
<td></td>
<td>30</td>
<td>30</td>
<td>dBc</td>
<td></td>
</tr>
<tr>
<td>TX Spectrum Mask for O-QPSK</td>
<td>Offset frequency &gt; 3.5 MHz, at 0 dBm output power</td>
<td>33</td>
<td>—</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Signal</td>
<td></td>
<td>—</td>
<td>25</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>TX Noise Floor</td>
<td></td>
<td>—</td>
<td>-126</td>
<td>dBm/Hz</td>
<td></td>
</tr>
</tbody>
</table>

FIGURE 10-1: EXAMPLE SPI SLAVE MODE TIMING

TABLE 10-5: EXAMPLE SPI SLAVE MODE REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>TssL2scH</td>
<td>CS ↓ to SCK ↑ Input</td>
<td>50</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>71</td>
<td>Tsch</td>
<td>SCK Input High Time</td>
<td>50</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>TscL</td>
<td>SCK Input Low Time</td>
<td>50</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>74</td>
<td>Tsch2oL</td>
<td>Hold Time of SDI Data Input to SCK Edge</td>
<td>25</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>TdoR</td>
<td>SDO Data Output Rise Time</td>
<td>—</td>
<td>25</td>
<td>ns</td>
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<td>76</td>
<td>TdoF</td>
<td>SDO Data Output Fall Time</td>
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<td>25</td>
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<td>78</td>
<td>TscR</td>
<td>SCK Output Rise Time (Master mode)</td>
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<td>80</td>
<td>Tsch2oDV, TscL2oDV</td>
<td>SDO Data Output Valid after SCK Edge</td>
<td>TBD</td>
<td>—</td>
<td>ns</td>
<td></td>
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<td>82</td>
<td>TssL2oDV</td>
<td>SDO Data Output Valid after CS ↓ Edge</td>
<td>TBD</td>
<td>—</td>
<td>ns</td>
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<td>83</td>
<td>TscL2ssH</td>
<td>CS ↑ after SCK Edge</td>
<td>50</td>
<td>—</td>
<td>ns</td>
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Legend: TBD = To Be Determined
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

40-Lead QFN

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<td>YYYYYYYYYYYY</td>
<td>YYYYYYYYYYYY</td>
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<tr>
<td>YYWWNNNN</td>
<td>YYWWNNNN</td>
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</table>

Example

![Symbol](MRF24J40.png)

MRF24J40
-I/MM 
0610017

Legend:

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<tr>
<th>XX...X</th>
<th>Product-specific information</th>
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<tr>
<td>Y</td>
<td>Year code (last digit of calendar year)</td>
</tr>
<tr>
<td>YY</td>
<td>Year code (last 2 digits of calendar year)</td>
</tr>
<tr>
<td>WW</td>
<td>Week code (week of January 1 is week '01')</td>
</tr>
<tr>
<td>NNN</td>
<td>Alphanumeric traceability code</td>
</tr>
<tr>
<td>63</td>
<td>Pb-free JEDEC designator for Matte Tin (Sn)</td>
</tr>
</tbody>
</table>

* This package is Pb-free. The Pb-free JEDEC designator (63) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
11.2 Package Details

The following sections give the technical details of the packages.

40-Lead Plastic Quad Flat, No Lead Package (MM) 6x6x0.9 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
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<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Contact Thickness</td>
<td>A3</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Contact Width</td>
<td>b</td>
</tr>
<tr>
<td>Contact Length §</td>
<td>L</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad §</td>
<td>K</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
APPENDIX A: LAYOUT AND PART SELECTION

A.1 Layout Considerations and RF Measurements

Below is an example of the circuit diagram of a balun. A balun is the impedance transformer from unbalanced input of the PCB antenna and the balanced input of the RF transceiver (pins RFP and RFN).

FIGURE A-1: EXAMPLE CIRCUIT DIAGRAM

![Circuit Diagram]

Figure A-2 shows the measured impedance of the balun where the center of the band is very close to 50Ω. When using low tolerance components (i.e., ±5%) along with an appropriate ground, the impedance will remain close to the 50Ω measurement. Figure A-3 shows the measured impedance of the PCB antenna using a logarithmic scale magnitude. Figure A-4 shows the same impedance using a Smith Chart diagram and Figure A-5 using a voltage standing wave ratio.

FIGURE A-2: MEASURED IMPEDANCE

![Measured Impedance Chart]
FIGURE A-3: IMPEDANCE OF THE PCB ANTENNA

FIGURE A-4: IMPEDANCE OF THE PCB ANTENNA IN SMITH CHART
The most critical part of maintaining proper impedance is adhering to the specified dimensions of the printed circuit board antenna (see Figure A-6). The antenna dimensions, if altered, will change the specified impedance. As an example, a 1 mm variance will shift the impedance by 5-10 MHz.

**FIGURE A-6: PRINTED CIRCUIT BOARD ANTENNA DIMENSIONS**

Note: This part has been simulated using a HFSS™ simulator provided by Ansoft Corporation.
Figure A-7 and Figure A-8 illustrate simulation results of this PCB antenna. Note the simulation results are very close to the measurements.

FIGURE A-7: SIMULATED PCB ANTENNA IMPEDANCE, XY PLOT
FIGURE A-8: SIMULATED PCB ANTENNA IMPEDANCE, SMITH PLOT

Ansoft Corporation
Smith Plot 1
Final Antenna ZigBee

27 Sep 2006
10:56:28

MP: 2.125 138.791
RX: -0.403 + j0.321
GB: 1.516 - j1.200
Q: 0.797
VSWR: 2.778
### A.2 PCB Layout Design

The printed circuit board is comprised of four basic FR4 layers: signal layout, RF ground, power line routing and ground (see Figure A-9). The guidelines will explain the requirements of these layers.

**FIGURE A-9: FOUR BASIC COPPER FR4 LAYERS**

- It is important to keep the original PCB thickness since any change will affect antenna performance (see total thickness of dielectric) or microstrip lines characteristic impedance.
- The first layer width of a 50Ω characteristic impedance microstrip line is 12 mils.
- Avoid having microstrip lines longer than 2.5 cm, since that line might get very close to a quarter wave length of the working frequency of the board which is 3.0 cm, and start behaving as an antenna.
- Except for the antenna layout, avoid sharp corners since they can act as an antenna. Round corners will eliminate possible future EMI problems.
- Digital lines by definition are prone to be very noisy when handling periodic waveforms and fast clock-switching rates. Avoid laying out a RF signal close to any digital lines.
- A via filled ground patch underneath the IC transceiver is mandatory.
- A power supply must be distributed to each pin in a star topology and low-ESR capacitors must be placed at each pin for proper decoupling noise.
- Decoupling each power pin is a tedious task, especially when the noise is affecting the performance of the transceiver in a specific bandwidth. Usually, low value caps (15-27 pF) combined with large value caps (100 nF) will cover a large spectrum of frequency.
- Passive components (inductors) must be in the high-frequency category and the SRF (Self-Resonant Frequency) should be at least two times higher than the operating frequency.

Figure A-10 and Figure A-11 illustrate the ground and power plane for the RF board.
FIGURE A-10: GROUND PLANE

FIGURE A-11: POWER GROUND PLANE

Note: See Figure A-6 for antenna dimensions
APPENDIX B: MRF24J40 SCHEMATIC AND BILL OF MATERIALS

B.1 Schematic

FIGURE B-1: MRF24J40 SCHEMATIC

Note:
Center pad on QFN package must be grounded.
## B.2 Bill of Materials

### TABLE B-1: MRF24J40 DAUGHTER CARD BILL OF MATERIALS

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Component Name</th>
<th>Reference Description</th>
<th>Value</th>
<th>Description</th>
<th>Vendor</th>
<th>Vendor #</th>
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<tbody>
<tr>
<td>1</td>
<td>CAP3528</td>
<td>C1</td>
<td>2.2 μF_Tant</td>
<td>Capacitor TANT, 2.2 μF, 25V, 10%, SMD</td>
<td>Kemet</td>
<td>T491B225K025AT</td>
</tr>
<tr>
<td>4</td>
<td>CAP0402</td>
<td>C23, C37, C38, C43</td>
<td>0.5 pF</td>
<td>CAP, Ceramic, 0.5 pF, 50V, NP0, 0402</td>
<td>Yageo America</td>
<td>0402CG508C9B200</td>
</tr>
<tr>
<td>2</td>
<td>CAP0402</td>
<td>C21, C54</td>
<td>20 pF</td>
<td>CAP, Ceramic, 20 pF, 50V, 5%, C0G, 0402</td>
<td>Murata Electronics</td>
<td>GRM1555C1H200JZ01D</td>
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<tr>
<td>4</td>
<td>CAP0402</td>
<td>C19, C44, C55, C58</td>
<td>27 pF</td>
<td>CAP, Ceramic, 27 pF, 50V, 0402, SMD</td>
<td>Panasonic - ECG</td>
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<td>C40</td>
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<td>J2</td>
<td>.100&quot; Socket/Terminal</td>
<td>Samtec</td>
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Revision A (December 2006)

Original data sheet for the MRF24J40 device.
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# Microchip Products

- [Microchip Internet Web Site](http://www.microchip.com)
- [IEEE 802.15.4](http://www.ieee802.org)
- [IEEE 802.15.4-2003](http://www.ieee802.org)
- [MRF24J40 Architecture](http://www.microchip.com)
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THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user’s guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip’s customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com
READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager
RE: Reader Response

From: Name ____________________________________________
       Company ____________________________________________
       Address ____________________________________________
       City / State / ZIP / Country ______________________________
       Telephone: (______) _________ - _________   FAX: (______) _________ - _________

Application (optional):

Would you like a reply? ___ Y  ___ N

Device: MRF24J40  Literature Number: DS39776A

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>XX</th>
<th>XXX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
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<tr>
<td>Temperature Range</td>
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<tr>
<td>Package</td>
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<td></td>
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<tr>
<td>Pattern</td>
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</tbody>
</table>

Example:

a) MRF24J40-I/MM: Industrial temperature, QFN package.

<table>
<thead>
<tr>
<th>Device</th>
<th>MRF24J40: IEEE 802.15.4™ 2.4 GHz RF Transceiver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Range</td>
<td>I = -40°C to +85°C (Industrial)</td>
</tr>
<tr>
<td>Package</td>
<td>MM = QFN (Plastic Quad Flat, No Lead)</td>
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</tbody>
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