Low Power RS485 Interface Transceiver

FEATURES

- Low Power: I_{CC} = 300μA Typ
- Designed for RS485 Interface Applications
- Single 5V supply
- –7V to 12V Bus Common-Mode Range Permits ±7V Ground Difference Between Devices on the Bus
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or with the Power Off
- Combined Impedance of a Driver Output and Receiver Allows Up to 32 Transceivers on the Bus
- 70mV Typical Input Hysteresis
- 30ns Typical Driver Propagation Delays with 5ns Skew
- Pin Compatible with the SN75176A, DS75176A and μA96176

APPLICATIONS

- Low Power RS485/RS422 Transceiver
- Level Translator

DESCRIPTION

The LTC485 is a low power differential bus/line transceiver designed for multipoint data transmission standard RS485 applications with extended common-mode range (12V to –7V). It also meets the requirements of RS422.

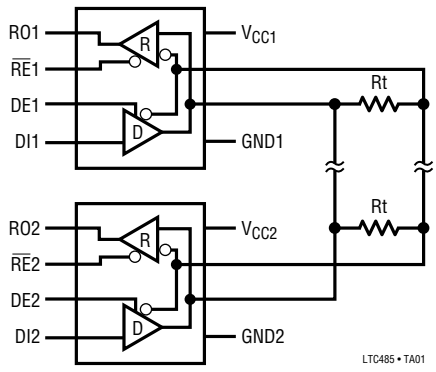
The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload of ESD damage.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common-mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state.

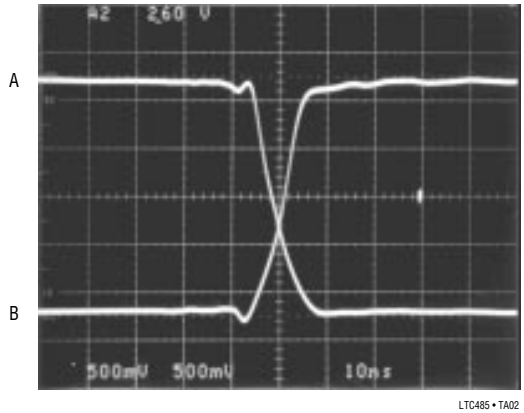
The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open.

The LTC485 is fully specified over the commercial and extended industrial temperature range.

TYPICAL APPLICATION



Driver Outputs

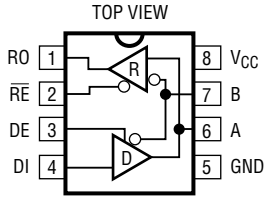


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 12V
Control Input Voltages ..... −0.5V to V_{CC} + 0.5V
Driver Input Voltage ..... −0.5V to V_{CC} + 0.5V
Driver Output Voltage ..... ±14V
Receiver Input Voltage ..... ±14V
Receiver Output Voltages ..... −0.5V to V_{CC} + 0.5V
Operating Temperature Range
LTC485I ..... −40°C ≤ T_A ≤ 85°C
LTC485C ..... 0°C ≤ T_A ≤ 70°C
LTC485M ..... −55°C ≤ T_A ≤ 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 155°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 100°C, θ_{JA} = 170°C/W (S)

ORDER PART NUMBER
LTC485CJ8 LTC485CN8 LTC485CS8 LTC485IN8 LTC485IS8 LTC485MJ8
S8 PART MARKING
485 485I

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, unless otherwise noted. (Notes 2 and 3)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	I_O = 0		●			5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 50Ω (RS422) R = 27Ω (RS485), Figure 1		● ●	2 1.5		 5	V V
ΔV_{OD}	Change in Magnitude of Driver DifferentialOutput Voltage for Complementary States	R = 27Ω or R = 50Ω, Figure 1		●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	R = 27Ω or R = 50Ω, Figure 1		●			3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary States	R = 27Ω or R = 50Ω, Figure 1		●			0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$		●	2			V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$		●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$		●			±2	µA
I_{IN2}	Input Current (A, B)	DE = 0, V_{CC} = 0V or 5.25V	V_{IN} = 12V	●			±1	mA
			V_{IN} = −7V	●			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver	−7V ≤ V_{CM} ≤ 12V		●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V		●		70		mV
V_{OH}	Receiver Output High Voltage	I_O = −4mA, V_{ID} = 200mV		●	3.5			V
V_{OL}	Receiver Outpu Low Voltage	I_O = 4mA, V_{ID} = −200mV		●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, 0.4V ≤ V_O ≤ 2.4V		●			±1	µA
R_{IN}	Receiver Input Resistance	−7V ≤ V_{CM} ≤ 12V		●	12			kΩ
I_{CC}	Supply Current	No Load, Pins 2, 3, 4 = 0V or 5V	Outputs Enabled	●		500	900	µA
			Outputs Disabled	●		300	500	µA
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = HIGH	V_O = −7V		●	35	100	250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = LOW	V_O = 10V		●	35	100	250	mA
I_{OSR}	Receiver Short-Circuit Current	0V ≤ V_O ≤ V_{CC}		●	7		85	mA

SWITCHING CHARACTERISTICS

V_{CC} = 5V ±5%, unless otherwise noted. (Notes 2 and 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3 and 5)	●	10	30	50	ns
t_{PHL}	Driver Input to Output		●	10	30	50	ns
t_{SKEW}	Driver Output to Output		●		5	10	ns
t_r, t_f	Driver Rise or Fall Time		●	3	15	25	ns
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 4 and 6) S2 Closed	●		40	70	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 4 and 6) S1 Closed	●		40	70	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 4 and 6) S1 Closed	●		40	70	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 4 and 6) S2 Closed	●		40	70	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3 and 7)	●	30	90	200	ns
t_{PHL}			●	30	90	200	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew		●		13		ns
t_{ZL}	Receiver Enable to Output Low	C_{RL} = 15pF (Figures 2 and 8) S1 Closed	●		20	50	ns
t_{ZH}	Receiver Enable to Output High	C_{RL} = 15pF (Figures 2 and 8) S2 Closed	●		20	50	ns
t_{LZ}	Receiver Disable from Low	C_{RL} = 15pF (Figures 2 and 8) S1 Closed	●		20	50	ns
t_{HZ}	Receiver Disable from High	C_{RL} = 15pF (Figures 2 and 8) S2 Closed	●		20	50	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out ot device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: The LTC485 is guaranteed by design to be functional over a supply voltage range of 5V ±10%. Data sheet parameters are guaranteed over the tested supply voltage range of 5V ±5%.

TEST CIRCUITS

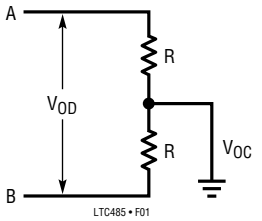


Figure 1. Driver DC Test Load

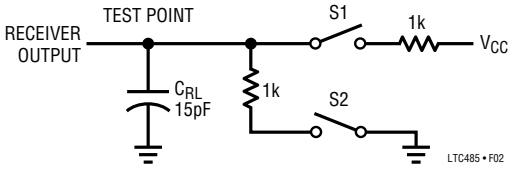


Figure 2. Receiver Timing Test Load

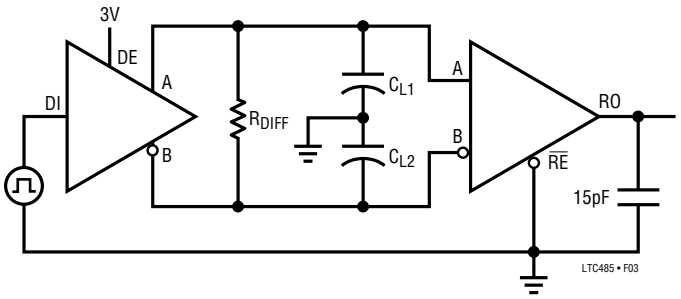


Figure 3. Driver/Receiver Timing Test Circuit

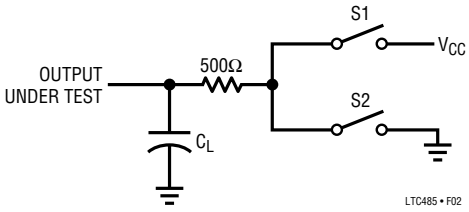


Figure 4. Driver Timing Test Load #2

SWITCHING TIME WAVEFORMS

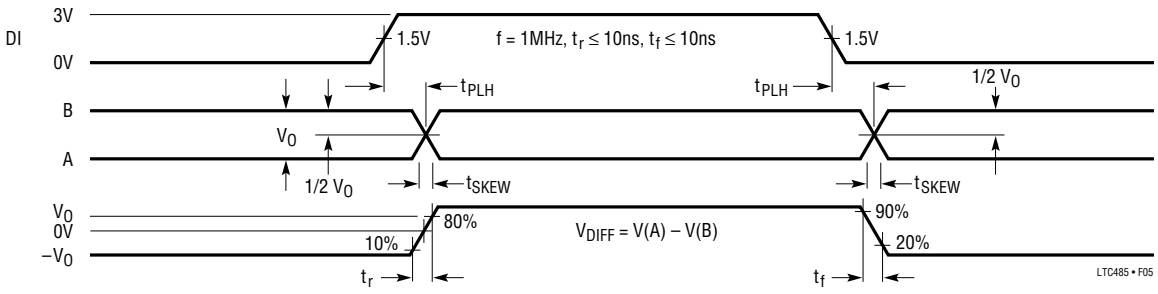


Figure 5. Driver Propagation Delays

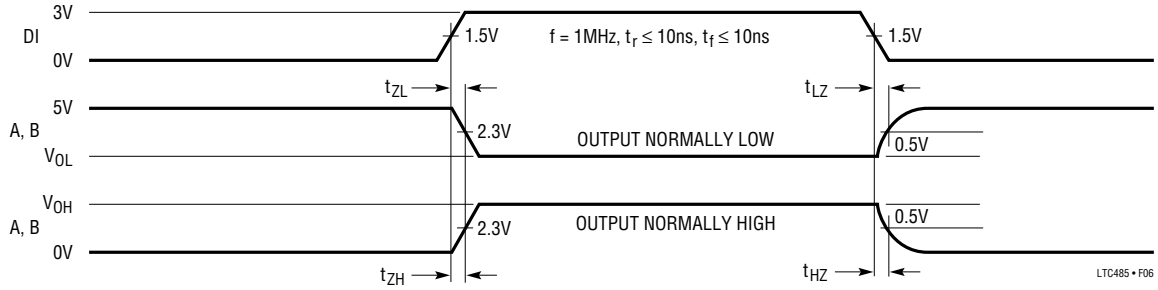


Figure 6. Driver Enable and Disable Times

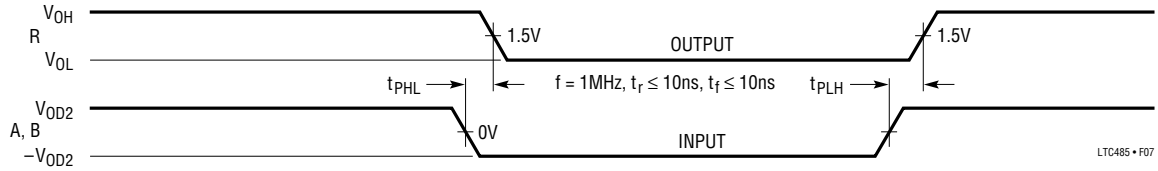


Figure 7. Receiver Propagation Delays

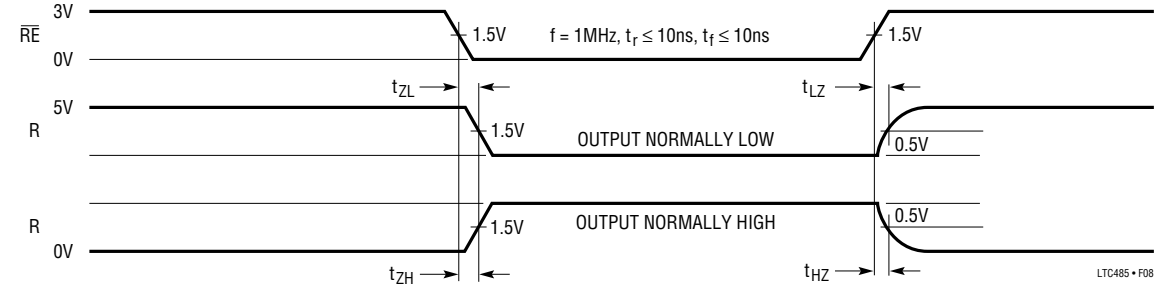


Figure 8. Receiver Enable and Disable Times

FUNCTION TABLES

LTC485 Transmitting

INPUTS			LINE CONDITION	OUTPUTS	
$\overline{RE}$	DE	DI		B	A
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

LTC485 Receiving

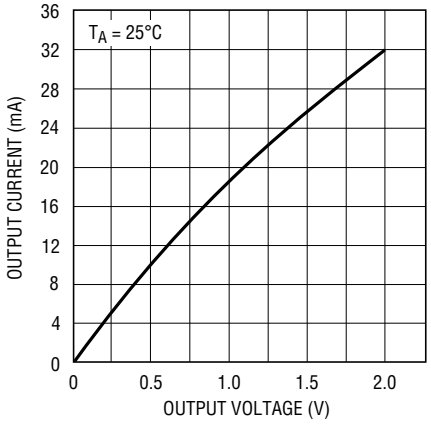
INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	R
0	0	≥0.2V	1
0	0	≤–0.2V	0
0	0	Inputs Open	1
1	0	X	Z

PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1	RO	Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then if A > B by 200mV, RO will be high. If A < B by 200mV, then RO will be low.
2	$\overline{RE}$	Receiver Output Enable. A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.
3	DE	Driver Outputs Enable. A high on DE enables the driver output. A and B, and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver.
4	DI	Driver Input. If the driver outputs are enabled (DE high), then a low on DI forces the outputs A low and B high. A high on DI with the driver outputs enabled will force A high and B low.
5	GND	Ground Connection.
6	A	Driver Output/Receiver Input.
7	B	Driver Output/Receiver Input.
8	V_{CC}	Positive Supply; 4.75 < V_{CC} < 5.25

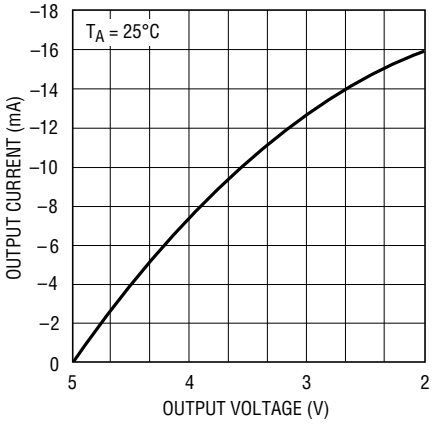
TYPICAL PERFORMANCE CHARACTERISTICS

Receiver Output Low Voltage vs Output Current



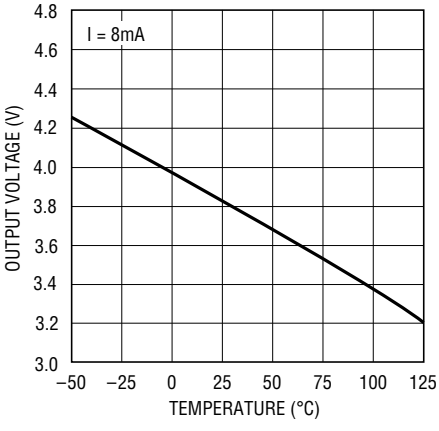
LTC485 • TPC01

Receiver Output High Voltage vs Output Current



LTC485 • TPC02

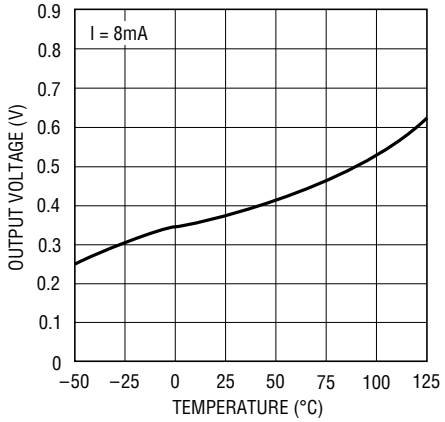
Receiver Output High Voltage vs Temperature



LTC485 • TPC03

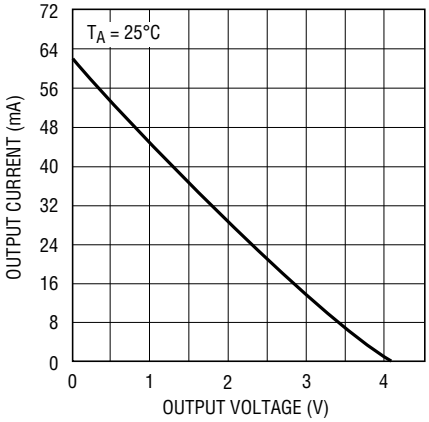
TYPICAL PERFORMANCE CHARACTERISTICS

Receiver Output Low Voltage vs Temperature



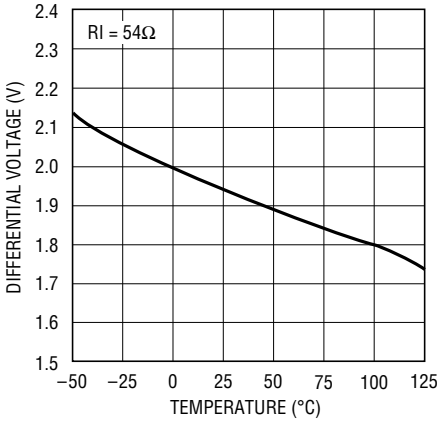
LTC485 • TPC03

Driver Differential Output Voltage vs Output Current



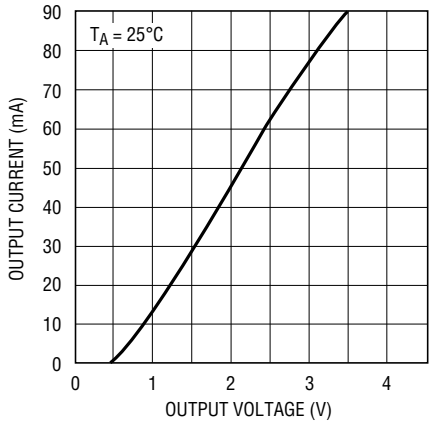
LTC485 • TPC05

Driver Differential Output Voltage vs Temperature



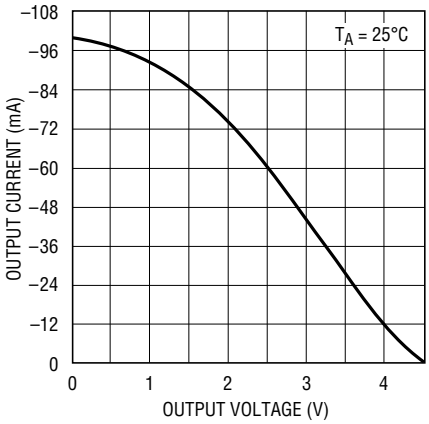
LTC485 • TPC06

Driver Output Low Voltage vs Output Current



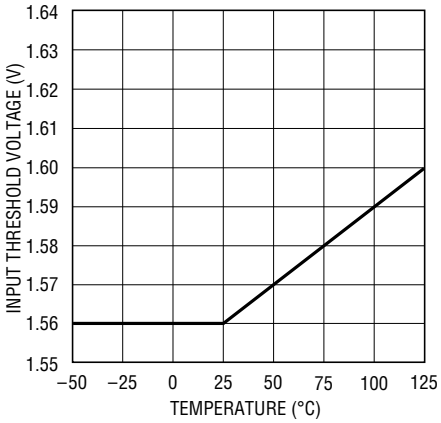
LTC485 • TPC07

Driver Output High Voltage vs Output Current



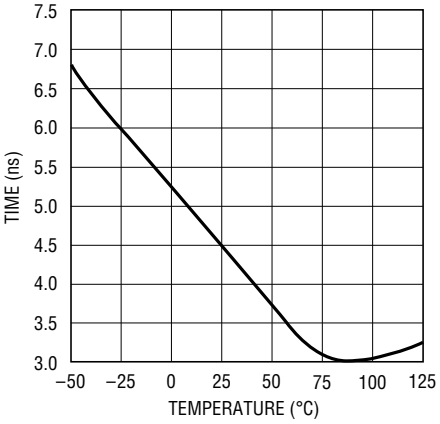
LTC485 • TPC08

TTL Input Threshold vs Temperature



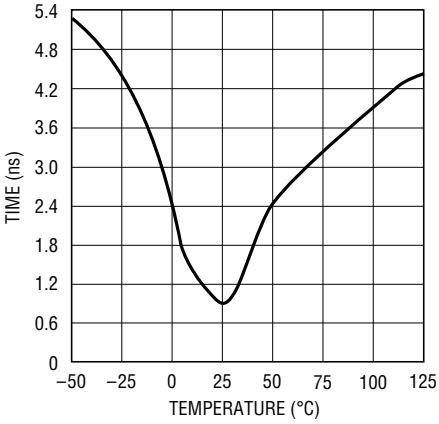
LTC485 • TPC09

Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



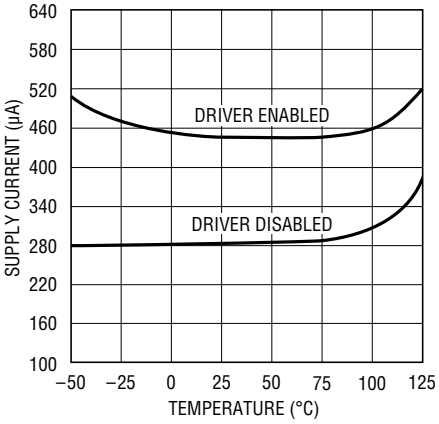
LTC485 • TPC10

Driver Skew vs Temperature



LTC485 • TPC11

Supply Current vs Temperature



LTC485 • TPC12

APPLICATIONS INFORMATION

Basic Theory of Operation

Previous RS485 transceivers have been designed using bipolar technology because the common-mode range of the device must extend beyond the supplies and the device must be immune to ESD damage and latchup. Unfortunately, the bipolar devices draw a large amount of supply current, which is unacceptable for the numerous applications that require low power consumption. The LTC485 is the first CMOS RS485/RS422 transceiver which features ultra-low power consumption without sacrificing ESD and latchup immunity.

The LTC485 uses a proprietary driver output stage, which allows a common-mode range that extends beyond the power supplies while virtually eliminating latchup and providing excellent ESD protection. Figure 9 shows the LTC485 output stage while Figure 10 shows a conventional CMOS output stage.

When the conventional CMOS output stage of Figure 10 enters a high impedance state, both the P-channel (P1) and the N-channel (N1) are turned off. If the output is then driven above V_{CC} or below ground, the P + /N-well diode (D1) or the N + /P-substrate diode (D2) respectively will turn on and clamp the output to the supply. Thus, the output stage is no longer in a high impedance state and is not able to meet the RS485 common-mode range requirement. In addition, the large amount of current flowing through either diode will induce the well known CMOS latchup condition, which could destroy the device.

The LTC485 output stage of Figure 9 eliminates these problems by adding two Schottky diodes, SD3 and SD4. The Schottky diodes are fabricated by a proprietary modification to the standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground, the parasitic diodes D1 or D2 still turn on, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or the substrate. Thus, the high impedance state is maintained even with the output voltage beyond the supplies. With no minority carrier current flowing into the N-well or substrate, latchup is virtually eliminated under power-up or power-down conditions.

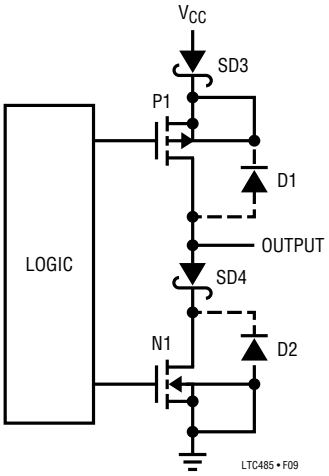


Figure 9. LTC485 Output Stage

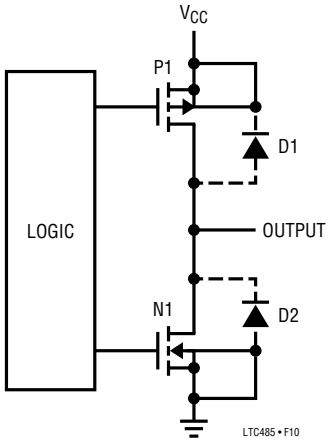


Figure 10. Conventional CMOS Output Stage

APPLICATIONS INFORMATION

The LTC485 output stage will maintain a high impedance state until the breakdown of the N-channel or P-channel is reached when going positive or negative respectively. The output will be clamped to either V_{CC} or ground by a Zener voltage plus a Schottky diode drop, but this voltage is way beyond the RS485 operating range. This clamp protects the MOS gates from ESD voltages well over 2000V. Because the ESD injected current in the N-well or substrate consists of majority carriers, latchup is prevented by careful layout techniques.

Propagation Delay

Many digital encoding schemes are dependent upon the difference in the propagation delay times of the driver and the receiver. Using the test circuit of Figure 13, Figures 11 and 12 show the typical LTC485 receiver propagation delay.

The receiver delay times are:

$$|t_{PLH} - t_{PHL}| = 9ns\ Typ,\ V_{CC} = 5V$$

The driver skew times are:

$$Skew = 5ns\ Typ,\ V_{CC} = 5V$$

$$10ns\ Max,\ V_{CC} = 5V,\ T_A = -40°C\ to\ 85°C$$

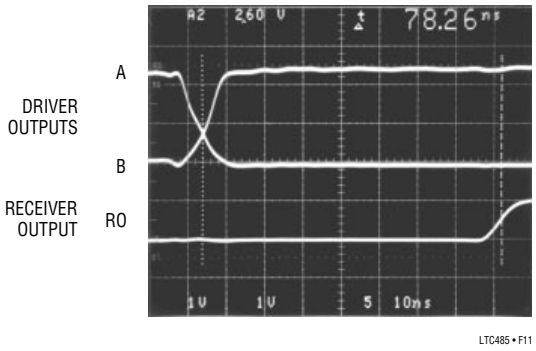


Figure 11. Receiver t_{PHL}

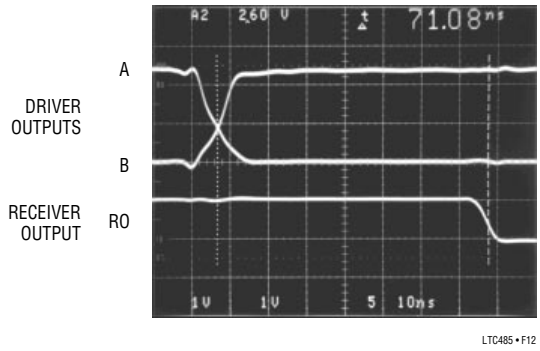


Figure 12. Receiver t_{PLH}

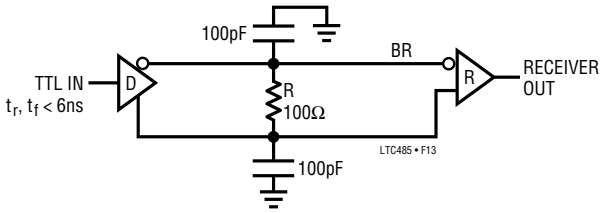


Figure 13. Receiver Propagation Delay Test Circuit

APPLICATIONS INFORMATION

LTC485 Line Length vs Data Rate

The maximum line length allowable for the RS422/RS485 standard is 4000 feet.

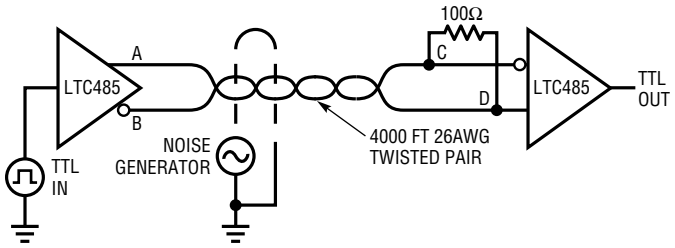


Figure 14. Line Length Test Circuit

Using the test circuit in Figure 14, Figures 15 and 16 show that with ~20V_{P-P} common-mode noise injected on the line, The LTC485 is able to reconstruct the data stream at the end of 4000 feet of twisted pair wire.

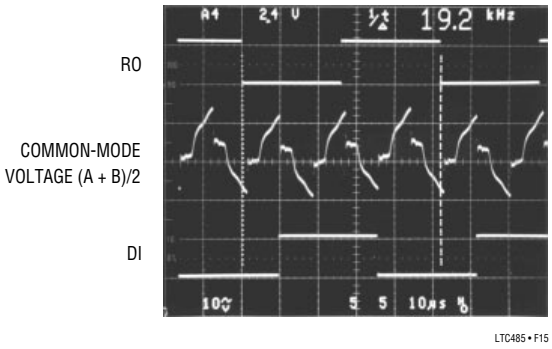


Figure 15. System Common-Mode Voltage at 19.2kHz

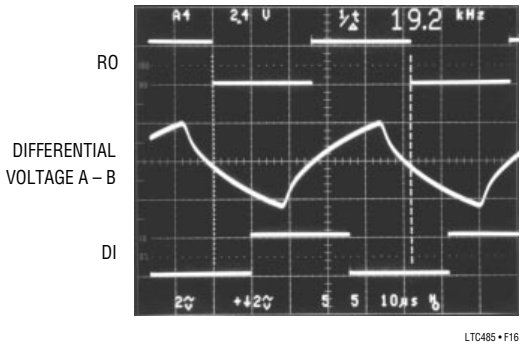


Figure 16. System Differential Voltage at 19.2kHz

Figures 17 and 18 show that the LTC485 is able to comfortably drive 4000 feet of wire at 110kHz.

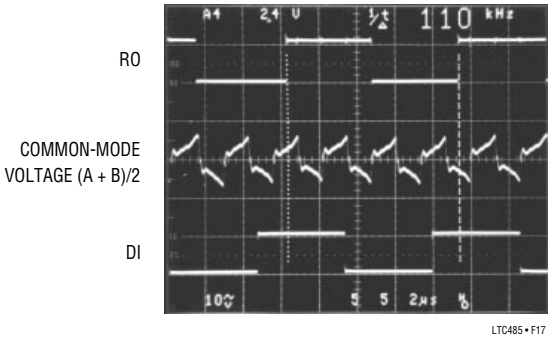


Figure 17. System Common-Mode Voltage at 110kHz

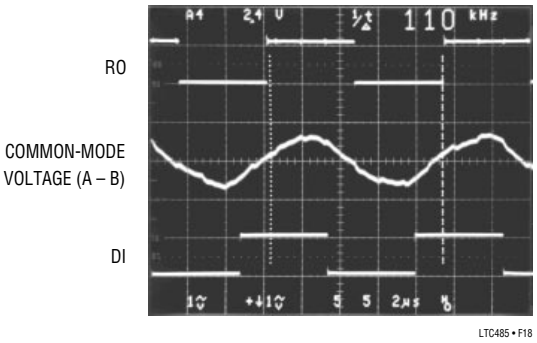


Figure 18. System Differential Voltage at 110kHz

When specifying line length vs maximum data rate the curve in Figure 19 should be used:

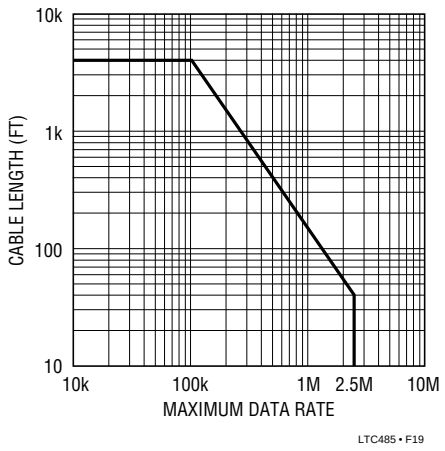
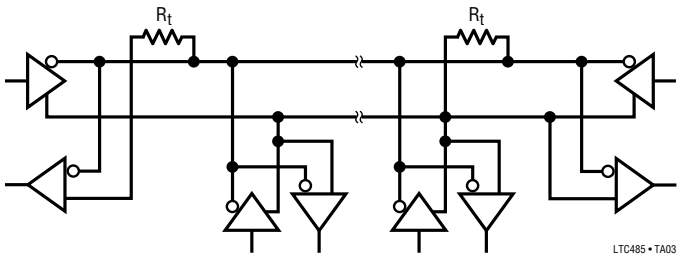


Figure 19. Cable Length vs Maximum Data Rate

TYPICAL APPLICATIONS

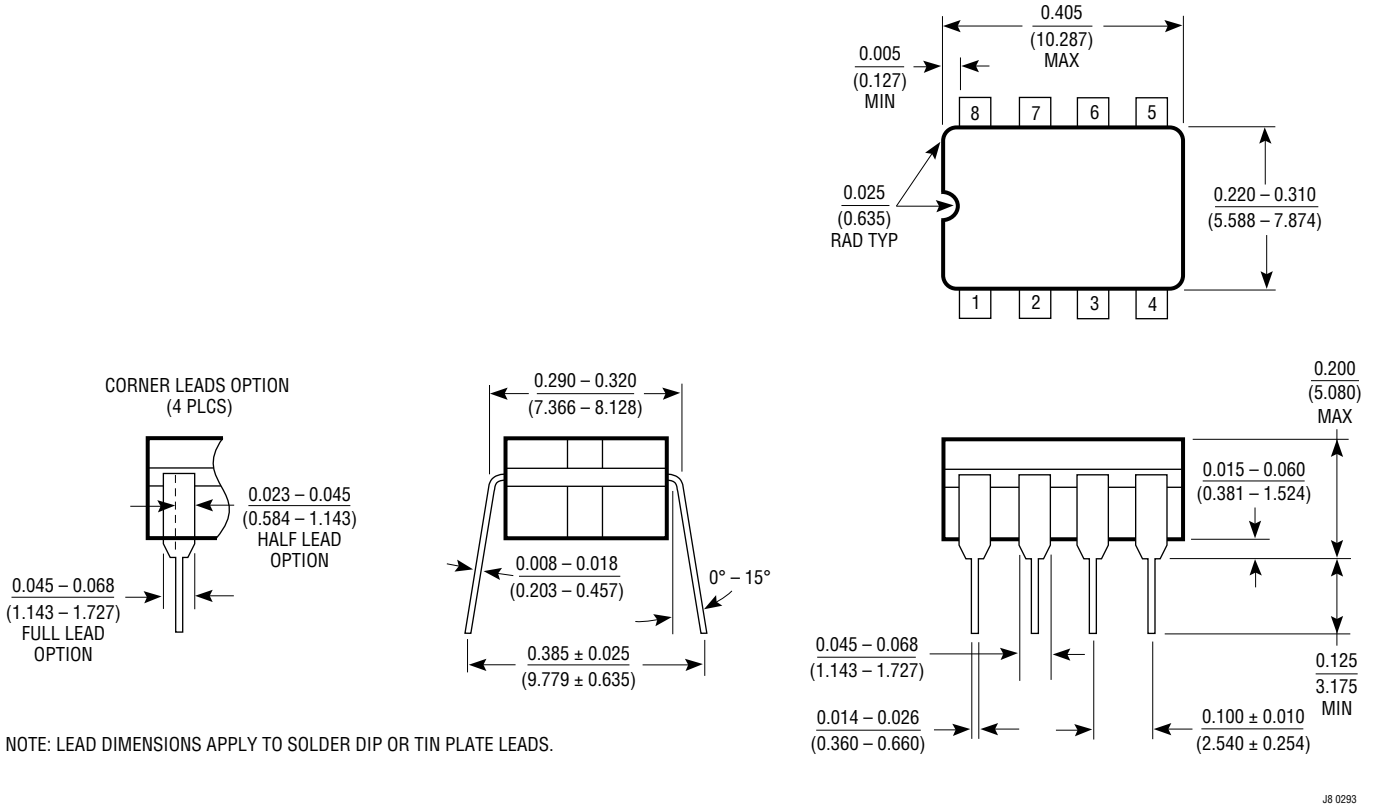
Typical RS485 Network



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

J8 Package
8-Lead Ceramic DIP



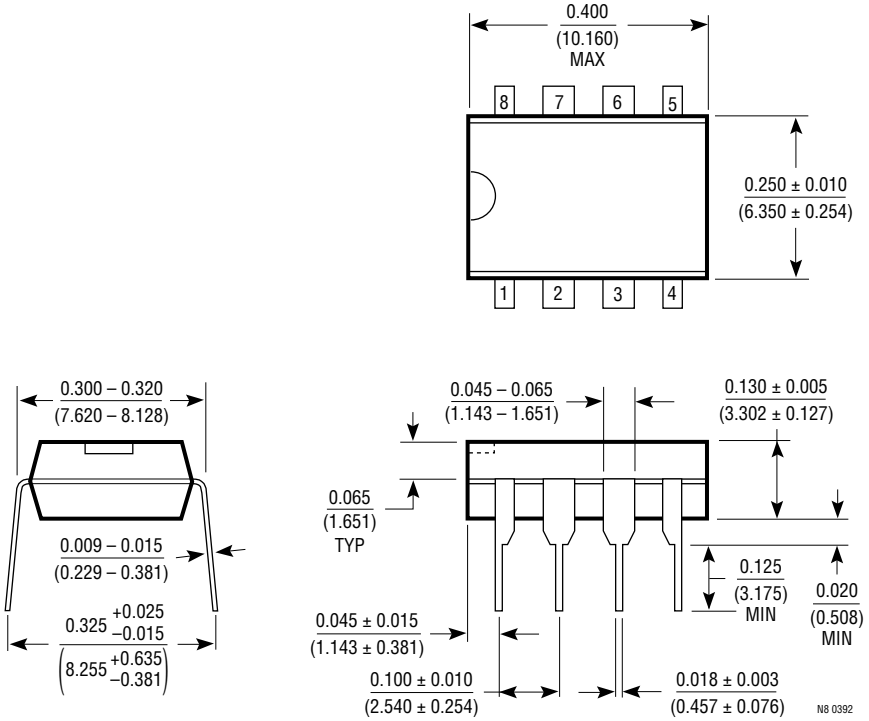
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

J8 0293

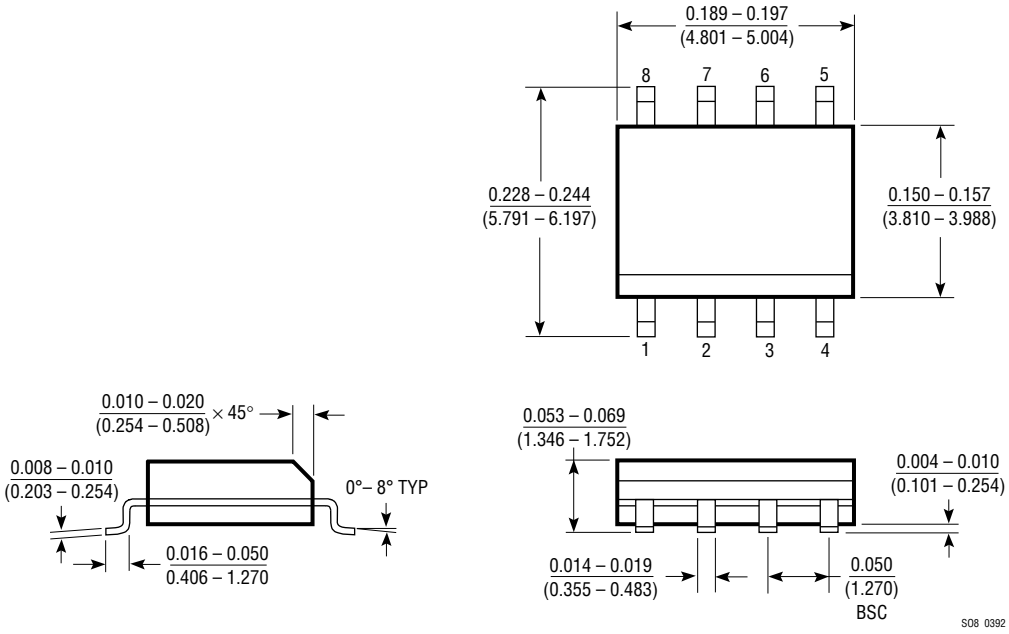
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



S8 Package
8-Lead Plastic SOIC



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