**General Description**

The LM1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative-going sync NTSC, PAL*, and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

**Features**

- AC coupled composite input signal
- > 10 kΩ input resistance
- < 10 mA power supply drain current
- Composite sync and vertical outputs
- Odd/even field output
- Burst gate/back porch output
- Horizontal scan rates to 150 kHz
- Edge triggered vertical output
- Default triggered vertical output for non-standard video signal (video games-home computers)

### Connection Diagram

![Connection Diagram](image)

Order Number LM1881M or LM1881N
See NS Package Number M08A or N08E

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*PAL in this datasheet refers to European broadcast TV standard “Phase Alternating Line”, and not to Programmable Array Logic.
### Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 13.2V
Input Voltage 3 Vpp (V\text{CC} ≤ 5V) 6 Vpp (V\text{CC} ≥ 8V)
Output Sink Currents; Pins 1, 3, 5 5 mA
Output Sink Current; Pin 7 2 mA
Package Dissipation (Note 1) 1100 mW
Operating Temperature Range 0°C – 70°C

Storage Temperature Range -65°C to +150°C
ESD Susceptibility (Note 2) 2 kV
Soldering Information
Dual-In-Line Package (10 sec.) 265°C
Small Outline Package Vapor Phase (60 sec.) 215°C
Infrared (15 sec.) 220°C
See AN-450 “Surface Mounting Methods and their Effect on Product Reliability” for other methods of soldering surface mount devices.

### Electrical Characteristics

\(V_{\text{CC}} = 5\text{V}; \text{R}_{\text{SET}} = 680 \text{k}\Omega; T_A = 25\text{C};\) Unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Tested Limit (Note 3)</th>
<th>Design Limit (Note 4)</th>
<th>Units (Limits)</th>
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</thead>
<tbody>
<tr>
<td>Supply Current</td>
<td>Outputs at Logic 1</td>
<td>(V_{\text{CC}} = 5\text{V})</td>
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<td></td>
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<td>1.8</td>
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<td>85</td>
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<td>Input Discharge Current</td>
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<td>(V_{\text{CC}} = 5\text{V})</td>
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<tr>
<td></td>
<td></td>
<td>(V_{\text{CC}} = 12\text{V})</td>
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<td>11.0</td>
<td>V\text{Max}</td>
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<tr>
<td></td>
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<td>(V_{\text{CC}} = 5\text{V})</td>
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<td>(V_{\text{CC}} = 12\text{V})</td>
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<td>V\text{Max}</td>
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<td>(V_{\text{CC}} = 5\text{V})</td>
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<td></td>
<td></td>
<td>90</td>
<td>\text{\mu\text{s}}\text{Max}</td>
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</table>

**Note 1:** For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 110°C/W, junction to ambient.

**Note 2:** ESD susceptibility test uses the “human body model, 100 pF discharged through a 1.5 k\Omega \text{ resistor}”.

**Note 3:** Typicals are at \(T_J = 25\text{C}\) and represent the most likely parametric norm.

**Note 4:** Tested Limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

**Note 5:** Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.

**Note 6:** Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5, and 7) to the \(R_{\text{SET}}\) pin (Pin 6).

**Note 7:** Delay time between the start of vertical sync (at input) and the vertical output pulse.
Typical Performance Characteristics

- **R_set Value Selection vs Vertical Serration Pulse Separation**
- **Vertical Default Sync Delay Time vs R_set**
- **Burst/Black Level Gate Time vs R_set**
- **Vertical Pulse Width vs R_set**
- **Vertical Pulse Width vs Temperature**
- **Supply Current vs Supply Voltage**

Note:Refer to the Vertical Sync Output section under Application Notes.
Application Notes

The LM1881 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5V (p-p) to 2V (p-p) can be accommodated. The LM1881 operates from a single supply voltage between 5V DC and 12V DC. The only required external components beside power supply and set current decoupling are the input coupling capacitor and a single resistor that sets internal current levels, allowing the LM1881 to be adjusted for source signals with line scan frequencies differing from 15.734 kHz. Four major sync signals are available from the I/C: composite sync including both horizontal and vertical scan timing information; a vertical sync pulse; a burst gate or back porch clamp pulse; and an odd/even output. The output of the R/S flip-flop goes to pin 3 and is biased 18 dB, effectively taking it below the comparator threshold. Consequently, the subcarrier content in the signal will be attenuated by almost 20 dB, effectively taking it below the comparator threshold. Filtering will also help if the source is contaminated with thermal noise. The output waveforms will become delayed from between 40 ns to as much as 200 ns due to this filter. This much delay will not usually be significant but it does contribute to the sync delay produced by any additional signal processing. Since the original video may also undergo processing, the need for time delay correction will depend on the total system, not just the sync stripper.

VERTICAL SYNC OUTPUT

A vertical sync output is derived by internally integrating the composite sync waveform (Figure 3). To understand the generation of the vertical sync pulse refer to the lower left hand section Figure 3. Note that there are two comparators in the section. One comparator has an internally generated voltage reference called V1 going to one of its inputs. The other comparator has an internally generated voltage reference called V2 going to one of its inputs. Both comparators have a common input at their noninverting input coming from the internal integrator. The internal integrator is used for integrating the composite sync signal. This signal comes from the input side of the composite sync buffer and are positive going sync pulses. The capacitor to the integrator is internal to the LM1881. The capacitor charge current is set by the value of the external resistor Rset. The output of the integrator is going to be at a low voltage during the normal horizontal lines because the integrator has a very short time to charge the capacitor, which is during the horizontal sync period. The equalization pulses will keep the output voltage of the integrator at about the same level, below the V1. During the vertical sync period the narrow positive going pulses shown in Figure 2 is called the serration pulse. The wide negative portion of the vertical sync period is called the vertical sync pulse. At the start of the vertical sync period, before the first serration pulse occurs, the integrator now charges the capacitor to a much higher voltage. At the first serration output the output should be between V1 and V2. This would give a high level at the output of the comparator with V1 as one of its inputs. This high is clocked into the “D” flip-flop by the falling edge of the serration pulse (remember the sync signal is inverted in this section of the LM1881). The “Q” output of the “D” flip-flop goes through the OR gate, and sets the R/S flip-flop. The output of the R/S flip-flop enables the internal oscillator and also clocks the ODD/EVEN “D” flip-flop. The ODD/EVEN field pulse operation is covered in the next section. The output of the oscillator goes to a divide by 8 circuit, thus resetting the R/S flip-flop after 8 cycles of the oscillator. The frequency of the oscillator is established by the internal capacitor going to the oscillator and the external Rset. The “D” output of the R/S flip-flop goes to pin 3 and is the actual vertical sync output of the LM1881. By clocking the “D” flip-flop at the start of the first serration pulse means that the vertical sync output pulse starts at this point in time and lasts for eight cycles of the internal oscillator as shown in Figure 2.

How Rset affects the integrator and the internal oscillator is shown under the Typical Performance Characteristics. The first graph is “Rset Value Selection vs Vertical Serration Pulse Separation”. For this graph to be valid, the vertical sync pulse should last for at least 85% of the horizontal half line (47% of a full horizontal line). A vertical sync pulse from any standard should meet this requirement; both NTSC and PAL do meet this requirement (the serration pulse is the remainder of the period, 10% to 15% of the horizontal...
FIGURE 2. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp

FIGURE 3
Rset with a video timing standard that has no serration pulse longer than the 30 μs voltage level V2. Since there is no falling edge at the end of the vertical sync period, then the falling edge of the vertical sync pulse at pin 3 of the LM1881. If the default vertical sync period ends before the end of the input vertical sync period, similar to starting the vertical sync pulse after the first serration pulse. A VGA standard is to be used as an example to show how this is done. In this standard, a horizontal line is 32 μs long. The vertical sync period is two horizontal lines long, or 64 μs. The vertical default sync delay time must be longer than the vertical sync period of 64 μs. In this case, Rset must be larger than 680 kΩ. Rset must still be small enough for the output of the integrator to reach V1 before the end of the vertical period of the input pulse. The first graph can be used to confirm that Rset is small enough for the integrator. Instead of using the vertical sync pulse separation, use the actual pulse width of the vertical sync period of NTSC (5 horizontal lines). A 550 kΩ will set the internal oscillator to a frequency such that eight cycles gives a time of 180 μs, just long enough to prevent a double vertical sync pulse at the vertical sync output of the LM1881.

The LM1881 also generates a default vertical sync pulse when the vertical sync period is unusually long and has no serration pulses. With a very long vertical sync time the integrator has time to charge its internal capacitor above the voltage level V2. Since there is no falling edge at the end of the vertical sync period, then the falling edge of the vertical sync pulse (positive pulse at the “D” flip-flop) will clock the high output from the comparator with V1 as a reference input. This will retrigger the oscillator, generating a second vertical sync output pulse. The “Vertical Default Sync Delay Time vs Rset” graph shows the relationship between the Rset value and the delay time from the start of the vertical sync period before the default vertical sync pulse is generated. Using the NTSC example again, the smallest resistor for Rset is 500 kΩ. The vertical default time delay is about 50 μs, much longer than the 30 μs serration pulse spacing.

A common question is how can one calculate the required Rset with a video timing standard that has no serration pulses during the vertical blanking. If the default vertical sync is to be used this is a very easy task. Use the “Vertical Default Sync Delay Time vs Rset” graph to select the necessary Rset to give the desired delay time for the vertical sync output signal. If a second pulse is undesirable, then check the “Vertical Pulse Width vs Rset” graph to make sure the vertical output pulse will extend beyond the end of the input vertical sync period. In most systems, the end of the vertical sync period may be very accurate. In this case the preferred design may be to start the vertical sync pulse at the end of the vertical sync period. Similar to starting the vertical sync pulse after the first serration pulse. A VGA standard is to be used as an example to show how this is done. In this standard, a horizontal line is 32 μs long. The vertical sync period is two horizontal lines long, or 64 μs. The vertical default sync delay time must be longer than the vertical sync period of 64 μs. In this case, Rset must be larger than 680 kΩ. Rset must still be small enough for the output of the integrator to reach V1 before the end of the vertical period of the input pulse. The first graph can be used to confirm that Rset is small enough for the integrator. Instead of using the vertical sync pulse separation, use the actual pulse width of the vertical sync period of NTSC, or 64 μs. In this example, a value of 1.0 μs is selected, well above the minimum of 680 kΩ. With this value for Rset, the pulse width of the vertical sync output pulse of the LM1881 is about 340 μs.

**ODD/EVEN FIELD PULSE**

An unusual feature of LM1881 is an output level from Pin 7 that identifies the video field present at the input to the LM1881. This can be useful in frame memory storage applications or in extracting test signals that occur only in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—i.e., at the bottom of the picture. This is called the “odd field” or “field 2.” The “even field” or “field 1” has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. Figure 3(a) shows the end of the even field and the start of the odd field. To detect the odd/even fields, the LM1881 again integrates the composite sync waveform (Figure 3). A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flipflop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this.
Application Notes (Continued)

threshold from being reached and the Q output of the flip-flop is toggled with each equalizing pulse. Since the half line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd/even field index is generated. Pin 7 remains low during the even field and high during the odd field.

BURST/BACKPORCH OUTPUT PULSE
In a composite video signal, the chroma burst is located on the backporch of the horizontal blanking period. This period, approximately 4.8 μs long, is also the black level reference for the subsequent video scan line. The LM1881 generates a pulse at Pin 5 that can be used either to retrieve the chroma burst from the composite video signal (thus providing a subcarrier synchronizing signal) or as a clamp for the DC restoration of the video waveform. This output is obtained simply by charging an internal capacitor starting on the trailing edge of the horizontal sync pulses. Simultaneously the output of Pin 5 is pulled low and held until the capacitor charge circuit times out—4 μs later. A shorter output burst gate pulse can be derived by differentiating the burst output using a series C-R network. This may be necessary in applications which require high horizontal scan rates in combination with normal (60–120 Hz) vertical scan rates.

APPLICATIONS
Apart from extracting a composite sync signal free of video information, the LM1881 outputs allow a number of interesting applications to be developed. As mentioned above, the burst gate/backporch clamp pulse allows DC restoration of the original video waveform for display or remodulation on an R.F. carrier, and retrieval of the color burst for color synchronization and decoding into R.G.B. components. For frame memory storage applications, the odd/even field level allows identification of the appropriate field ensuring the correct read or write sequence. The vertical pulse output is particularly useful since it begins at a precise time—the rising edge of the first vertical serration in the sync waveform. This means that individual lines within the vertical blanking period (or anywhere in the active scan line period) can easily be extracted by counting the required number of transitions in the composite sync waveform following the start of the vertical output pulse.

The vertical blanking interval is proving popular as a means to transmit data which will not appear on a normal T.V. receiver screen. Data can be inserted beginning with line 10 (the first horizontal scan line on which the color burst appears) through to line 21. Usually lines 10 through 13 are not used which leaves lines 14 through 21 for inserting signals, which may be different from field to field. In the U.S., line 19 is normally reserved for a vertical interval reference signal (VIRS) and line 21 is reserved for closed caption data for the hearing impaired. The remaining lines are used in a number of ways. Lines 17 and 18 are frequently used during studio processing to add and delete vertical interval test signals (VITS) while lines 14 through 18 and line 20 can be used for Videotex/Teletext data. Several institutions are proposing to transmit financial data on line 17 and cable systems use the available lines in the vertical interval to send decoding data for descrambler terminals.

Since the vertical output pulse from the LM1881 coincides with the leading edge of the first vertical serration, sixteen positive or negative transitions later will be the start of line 14 in either field. At this point simple counters can be used to select the desired line(s) for insertion or deletion of data.

VIDEO LINE SELECTOR
The circuit in Figure 4 puts out a single video line according to the binary coded information applied to line select bits b0–b7. A line is selected by adding two to the desired line number, converting to a binary equivalent and applying the result to the line select inputs. The falling edge of the LM1881’s vertical pulse is used to load the appropriate number into the counters (MM74C193N) and to set a start count latch using two NAND gates. Composite sync transitions are counted using the borrow out of the desired number of counters. The final borrow out pulse is used to turn on the analog switch (CD4066BC) during the desired line. The falling edge of this signal also resets the start count latch, thereby terminating the counting.

The circuit, as shown, will provide a single line output for each field in an interlaced video system (television) or a single line output in each frame for a non-interlaced video system (computer monitor). When a particular line in only one field of an interlaced video signal is desired, the odd/even field index output must be used instead of the vertical output pulse (invert the field index output to select the required field). A single counter is needed for selecting lines 3 to 14; two counters are needed for selecting lines 15 to 253; and three counters will work for up to 2046 lines. An output buffer is required to drive low impedance loads.

MULTIPLE CONTIGUOUS VIDEO LINE SELECTOR WITH BLACK LEVEL RESTORATION
The circuit in Figure 5 will select a number of adjoining lines starting with the line selected as in the previous example. Additional counters can be added as described previously for either higher starting line numbers or an increased number of contiguous output lines. The back porch pulse output of the LM1881 is used to gate the video input’s black level through a low pass filter (10 kΩ, 10 μF) providing black level restoration at the video output when the output selected line(s) is not being gated through.
Typical Applications

FIGURE 4. Video Line Selector

FIGURE 5. Multiple Contiguous Video Line Selector With Black Level Restoration
Physical Dimensions inches (millimeters)

Molded Small Outline Package (M)
Order Number LM1881M
NS Package Number M08A

Molded Dual-In-Line Package (N)
Order Number LM1881N
NS Package Number N08E

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